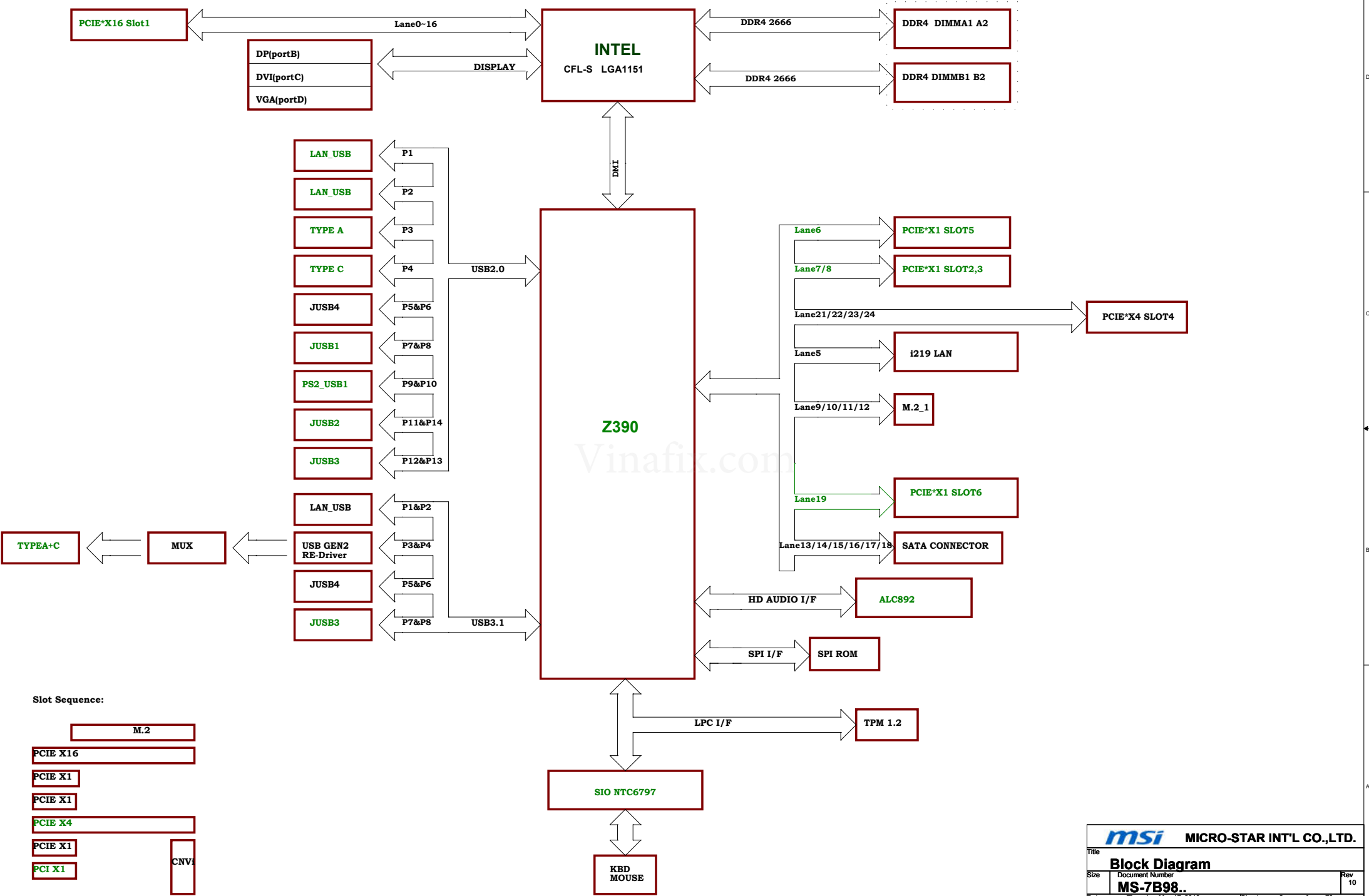
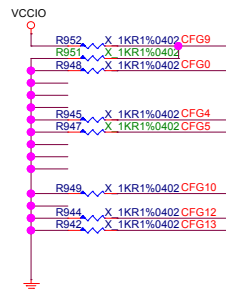
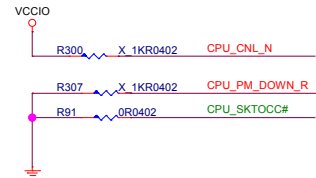
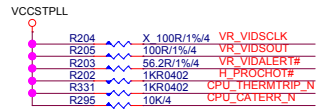


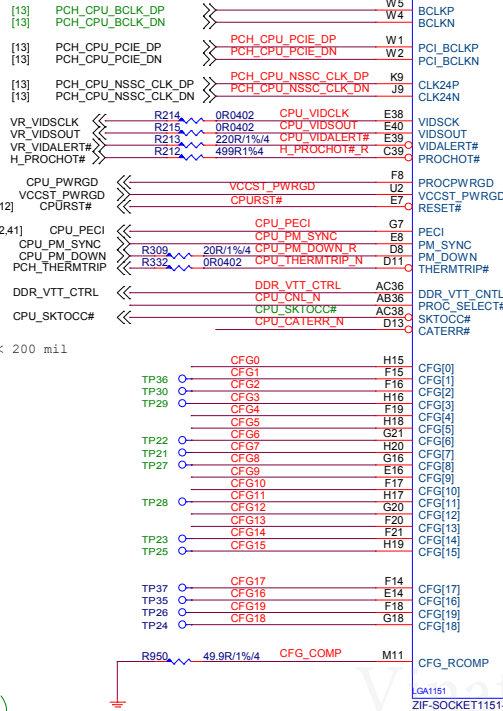
MS-7B98 Block Diagram



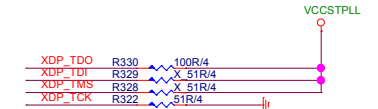
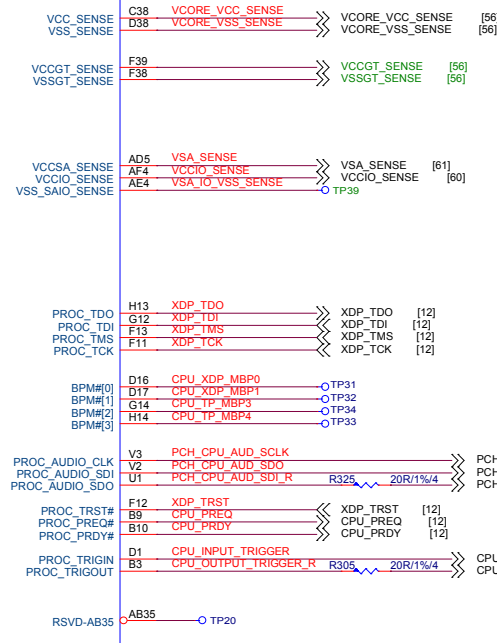


2017/7/13
Remove JP1 because JP1 combine to J1
Please see the D78 on page 54

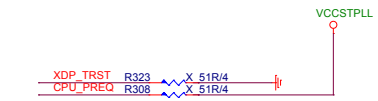
CPU_PM_DOWN_R < 200 mil



CPU1E CFL-S



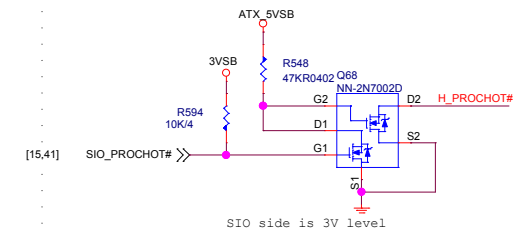
Close CPU <1100 mil
1000 mil < CPU_XDP_MBP0~1 < 6000 mil



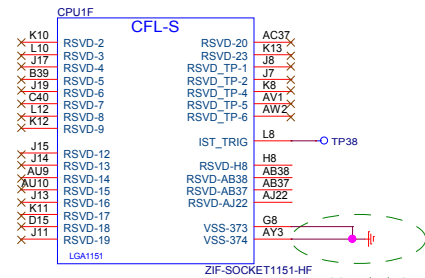
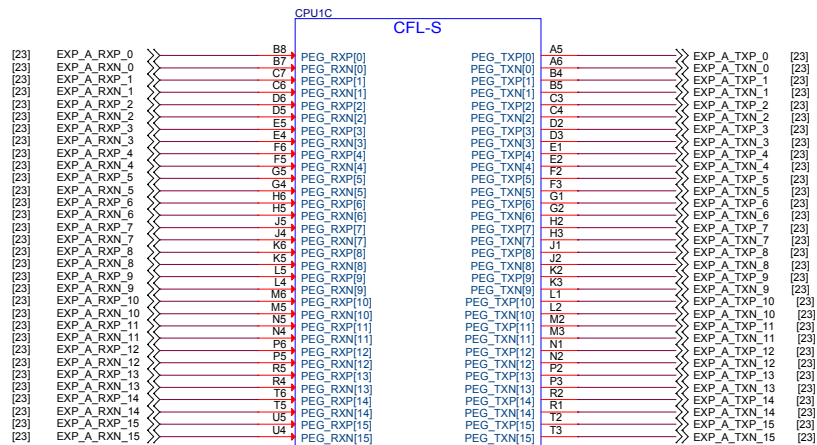
CFG Strap

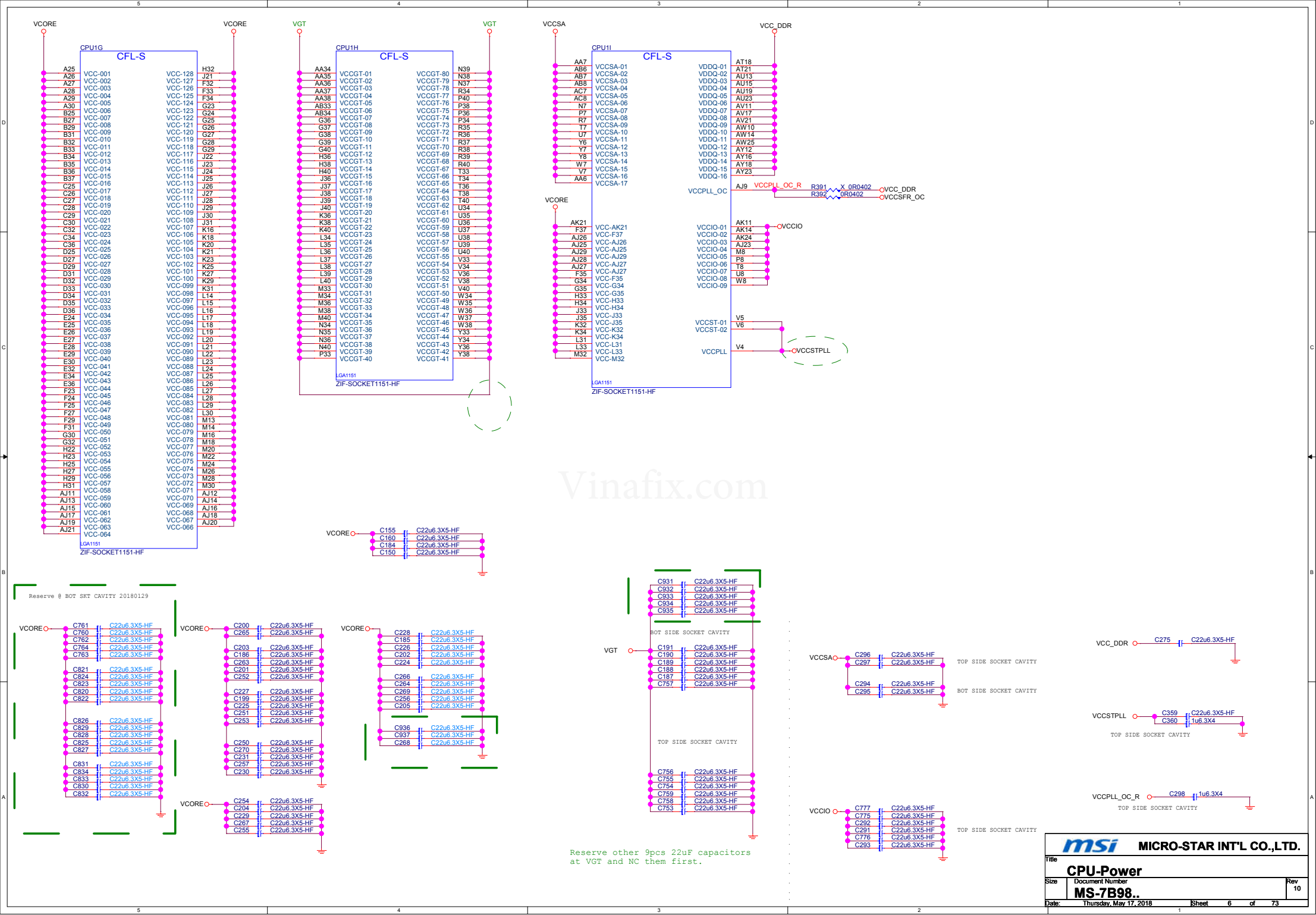
CFG Table

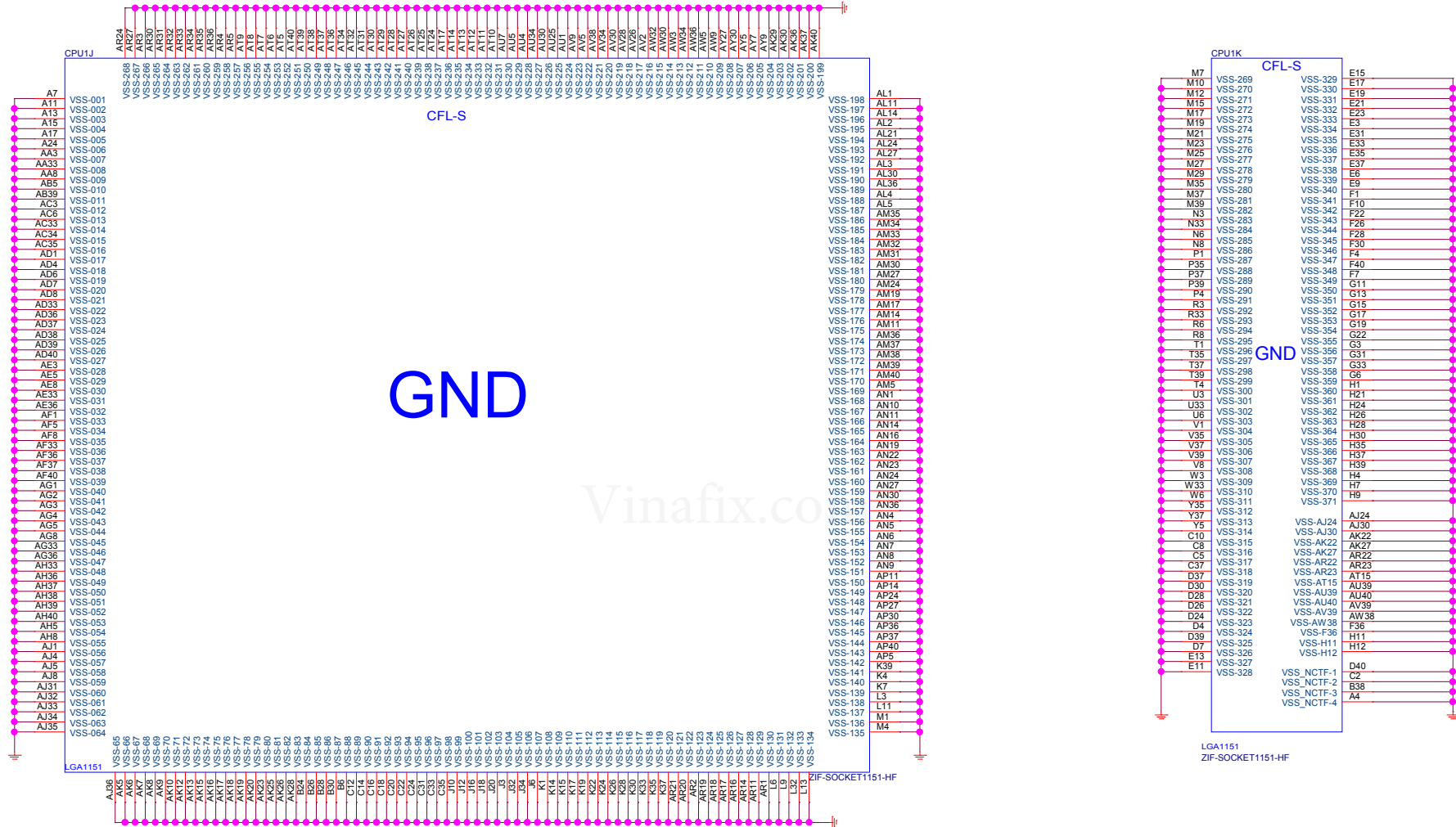
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEGCFGSEL[0]
6	DISABLE	ENABLE	PEGCFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

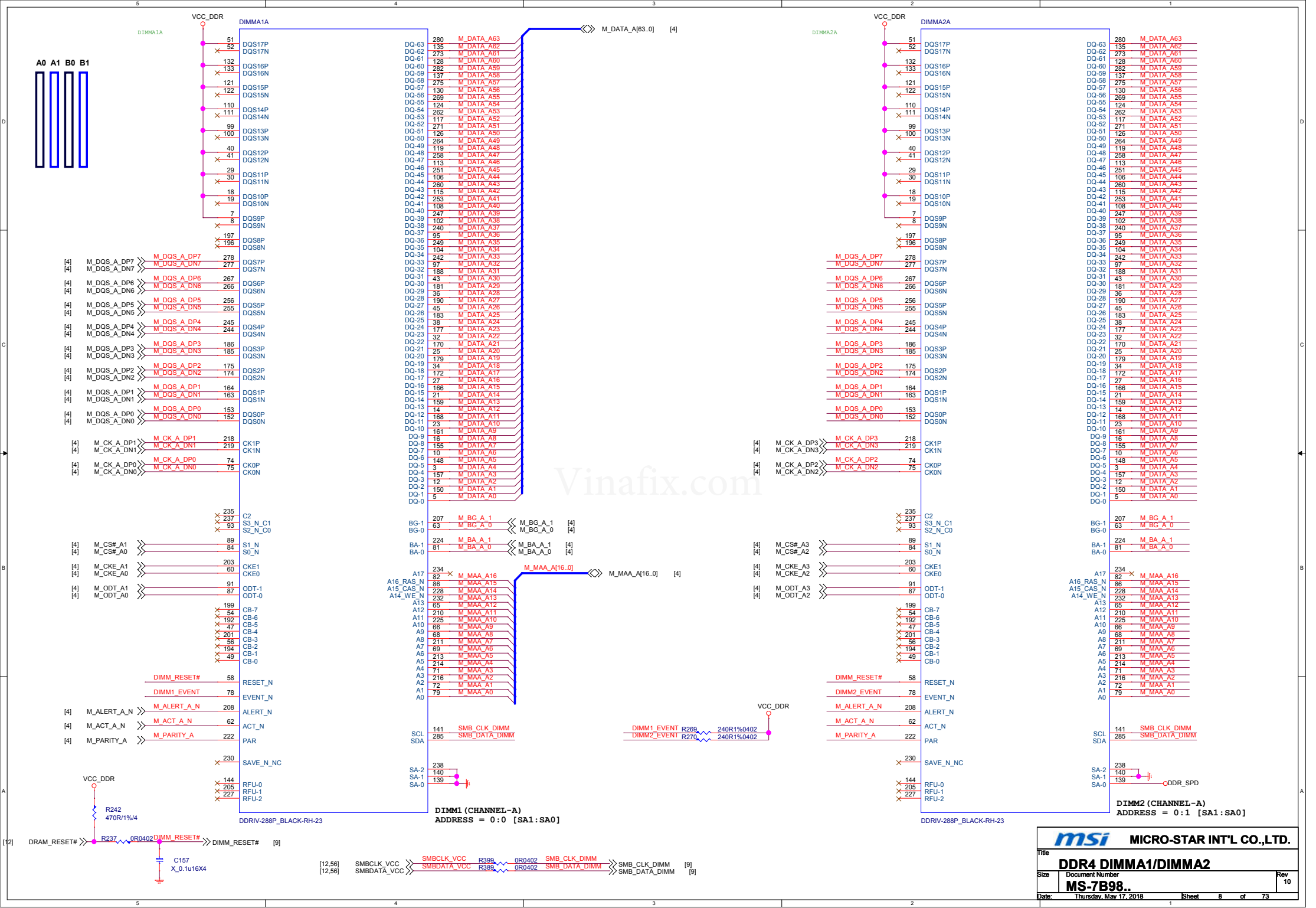


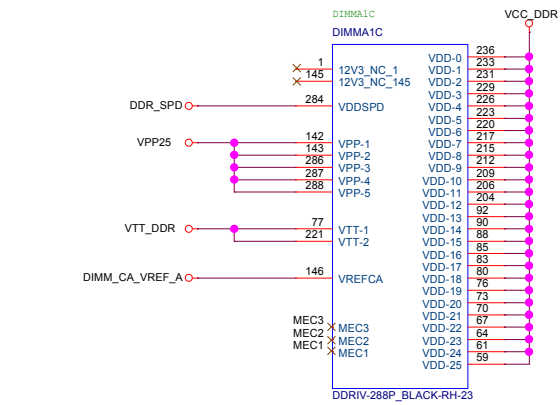
SIO side is 3V level



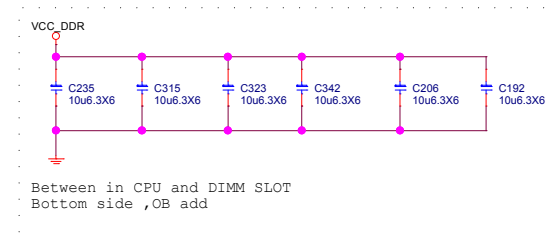
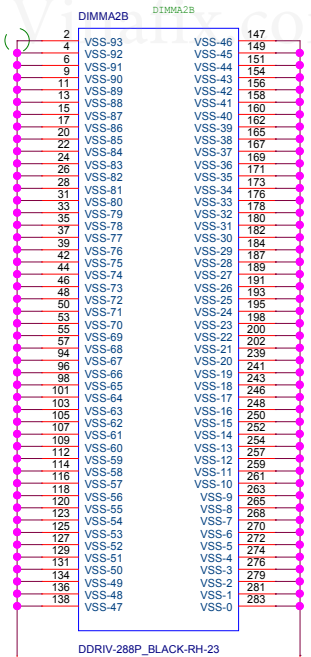
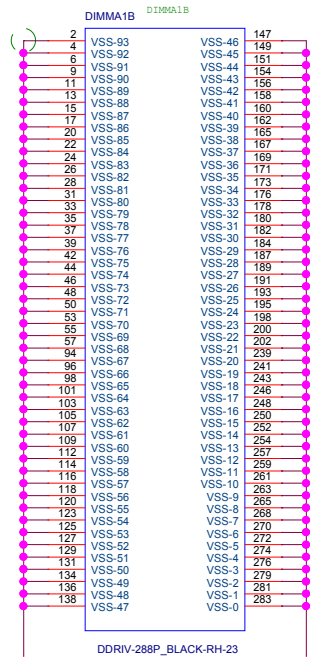
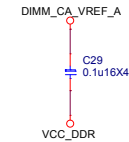
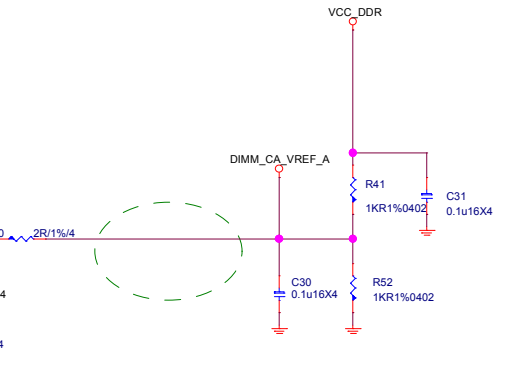
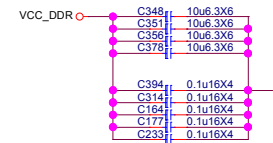
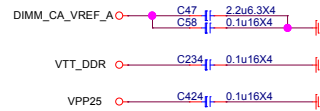
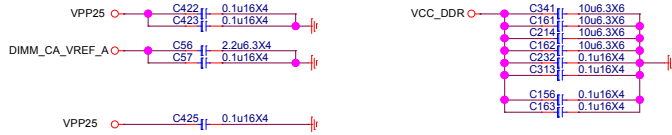
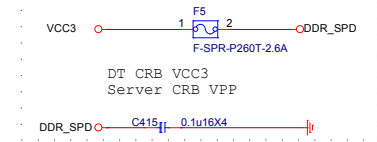
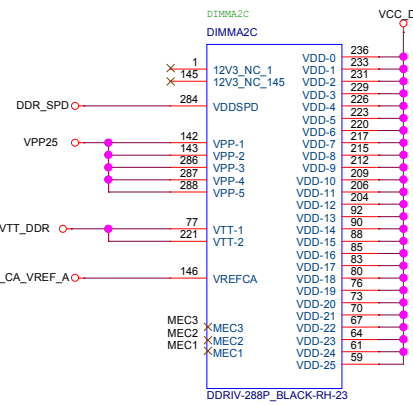
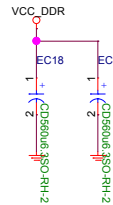


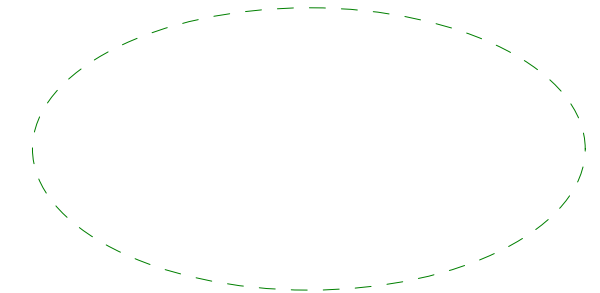
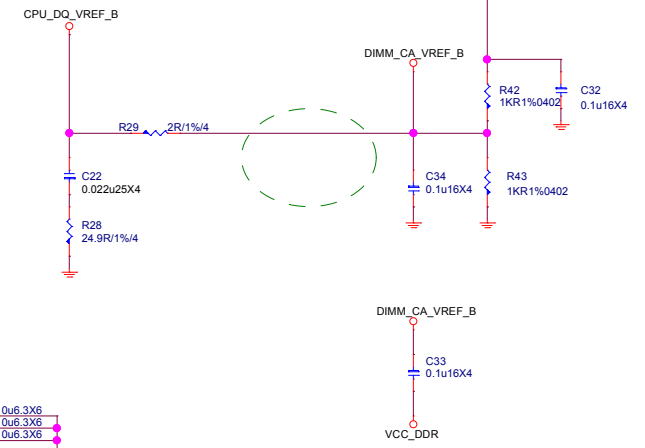
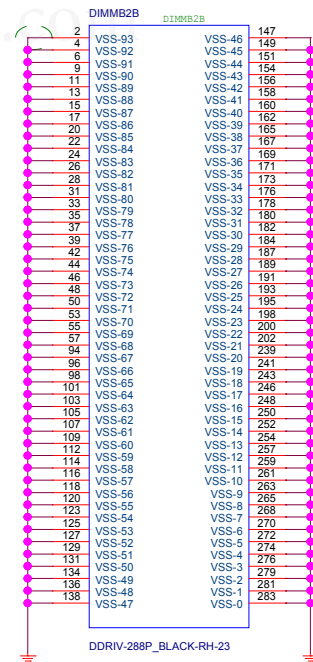
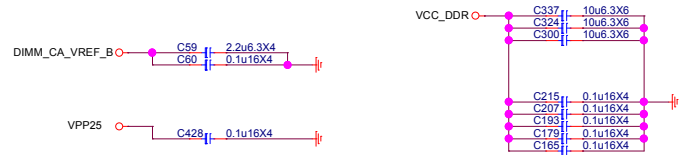
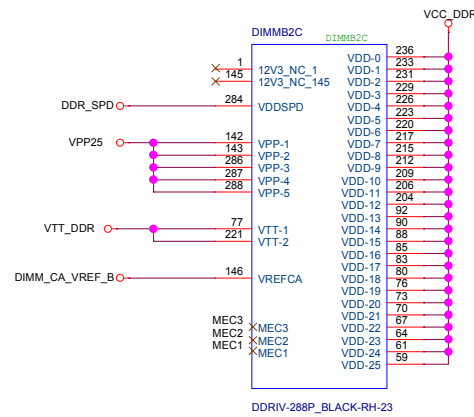
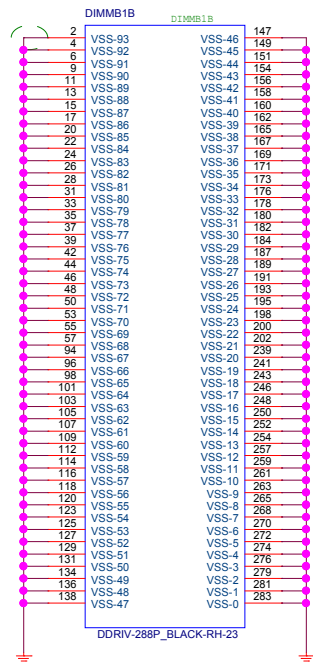
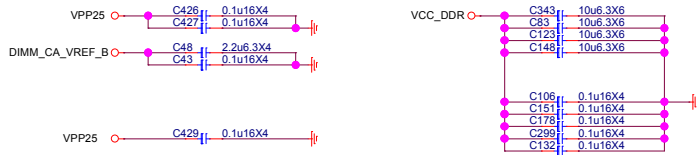
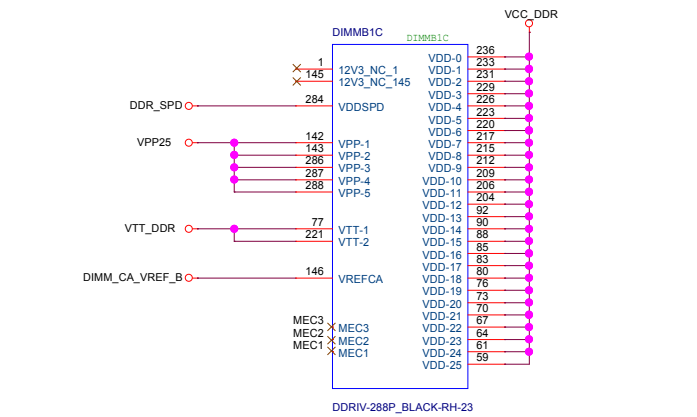


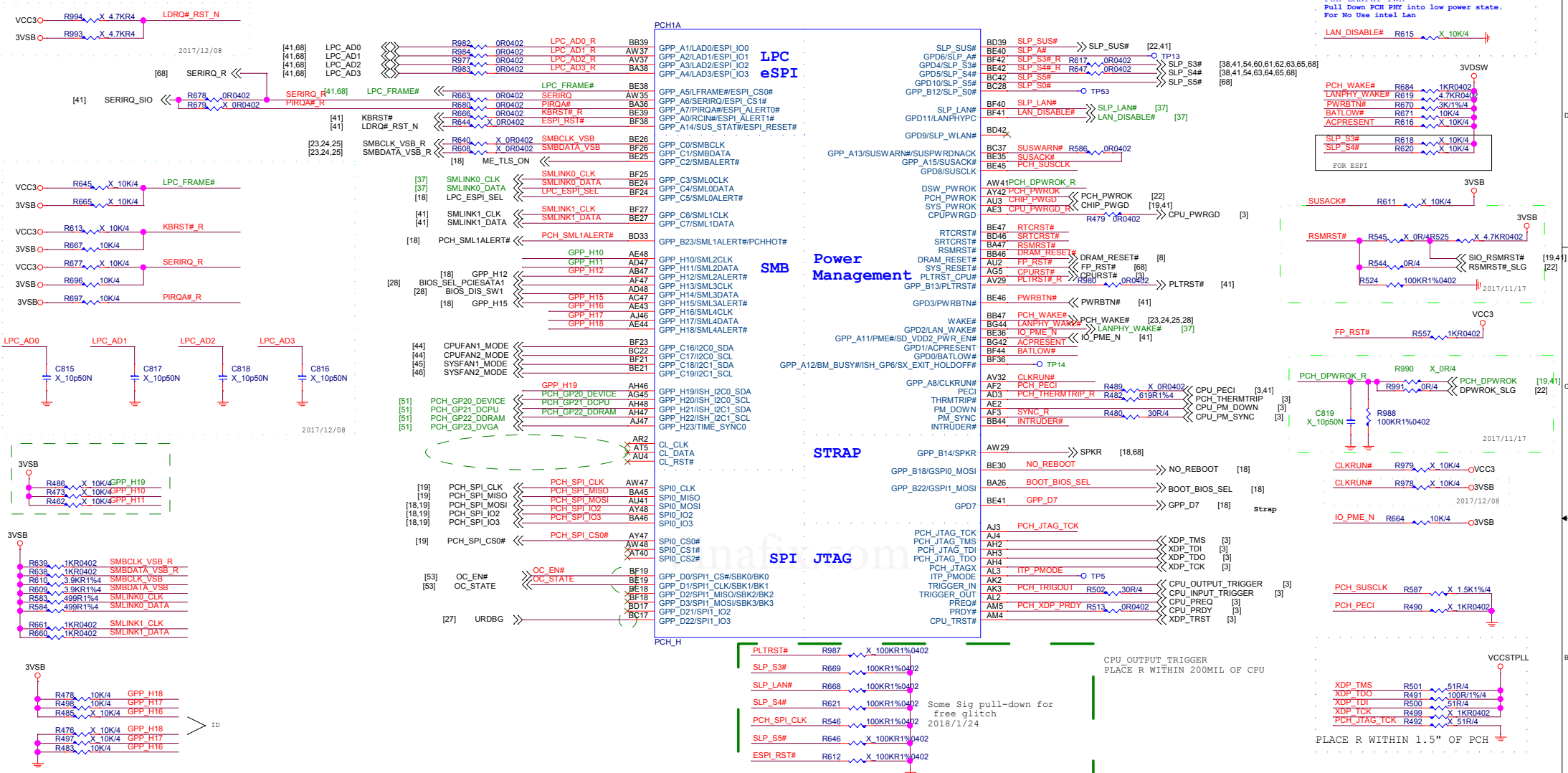




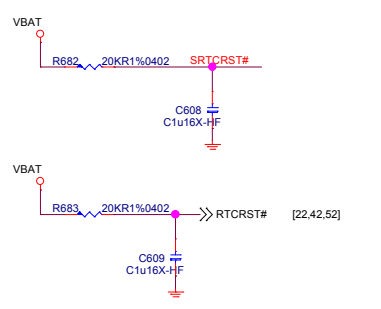
DIMM SLOT PN BY SPEC



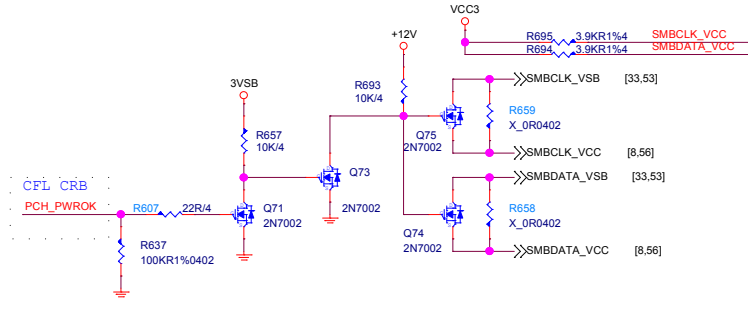
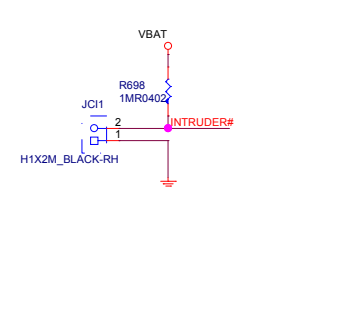




RTC

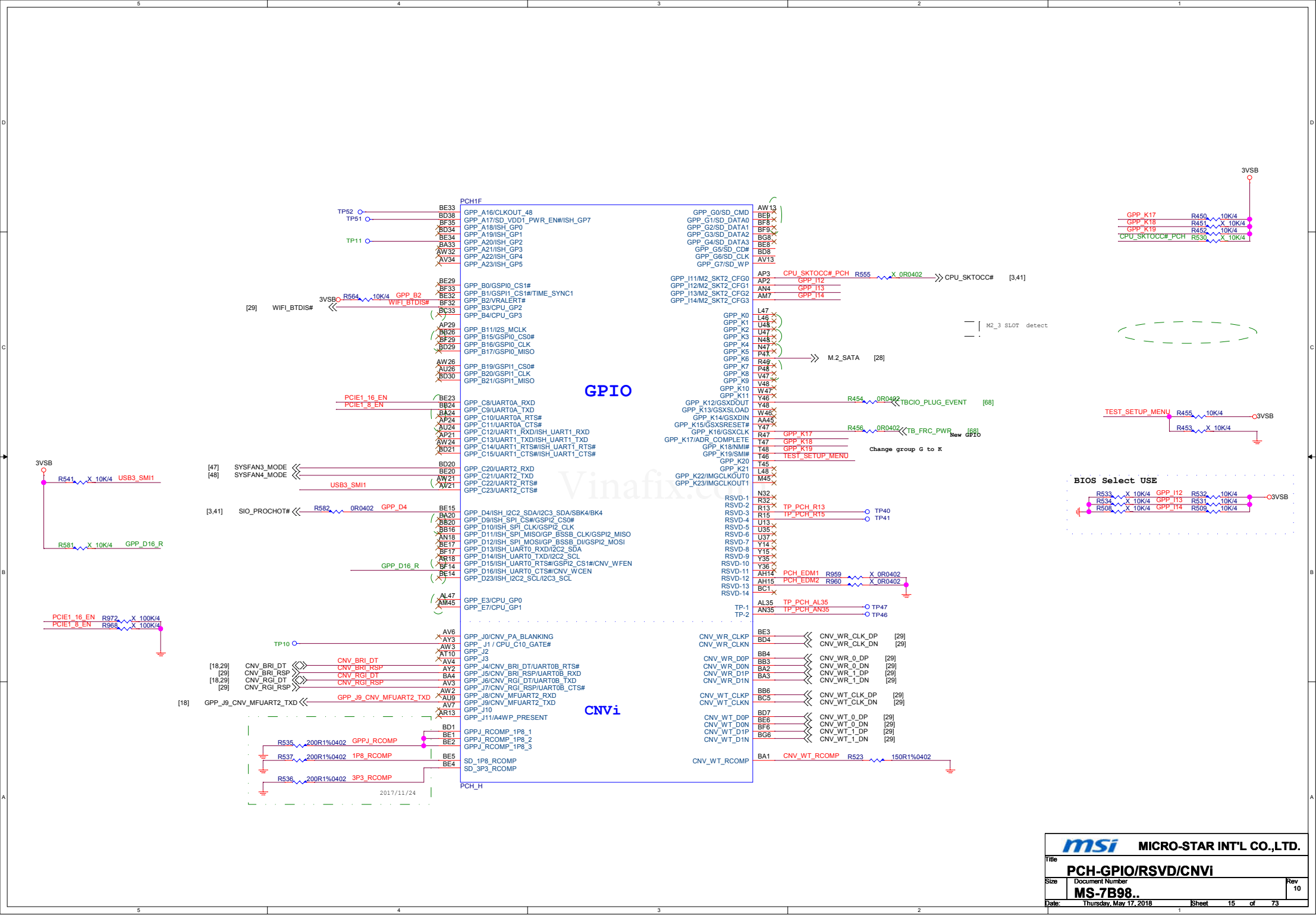


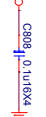
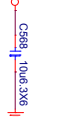
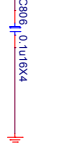
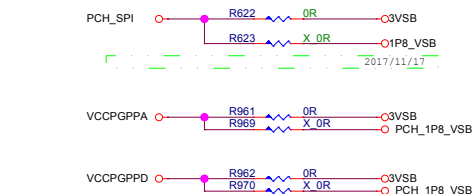
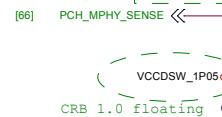
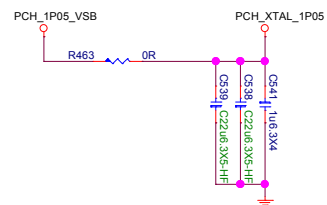
Chassis Intrusion



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Title		PCH-LPC/SPI/SMBUS/MISC	
Size	Document Number	Rev 10	
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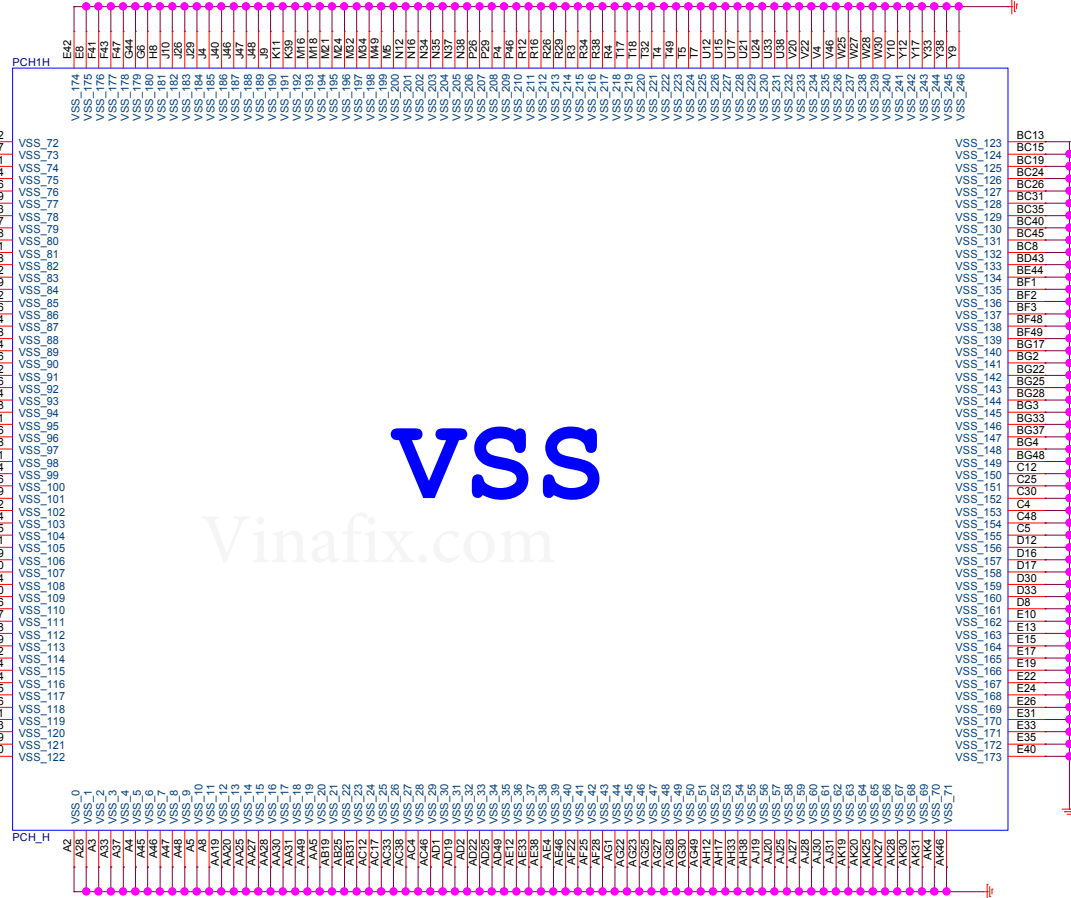




VSS

Vinafix.com

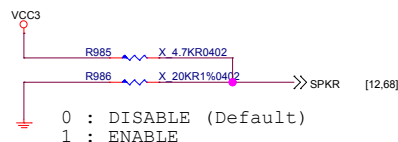
TP45



MICRO-STAR INT'L CO.,LTD.

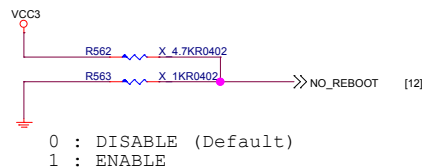
Title		PCH-GND
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TOP Swap



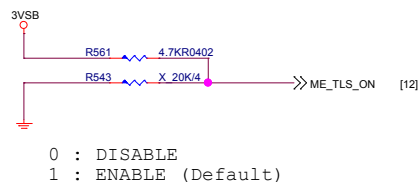
Internal pull-down is disabled after PCH_PWROK is high.

No Reboot



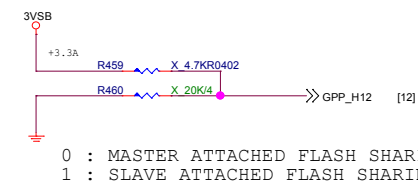
Internal pull-down is disabled after PCH_PWROK is high.

TLS confidentiality



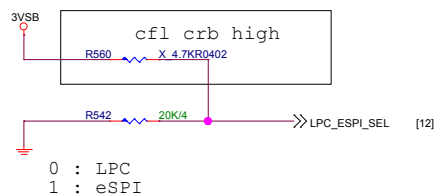
Internal pull-down is disabled after RSMRST# de-assert.

ESPI FLASH SHARING MODE



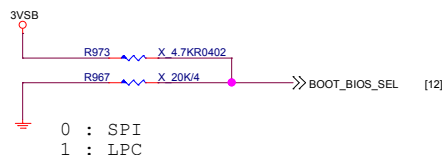
Internal pull-down is disabled after RSMRST# de-assert.

LPC eSPI Mode



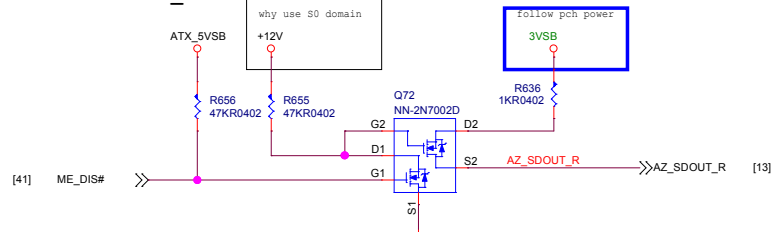
Internal pull-down is disabled after RSMRST# de-assert.

Boot BIOS



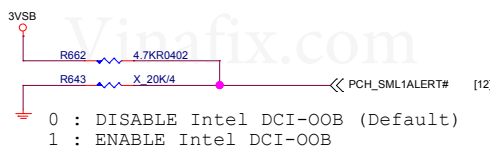
Internal pull-down is disabled after PCH_PWROK is high.

HDA_SDO



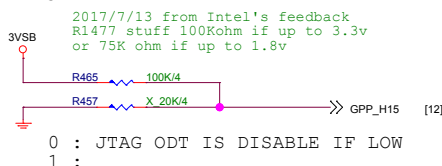
Internal pull-down is disabled after PCH_PWROK is high.

DCI ENABLE



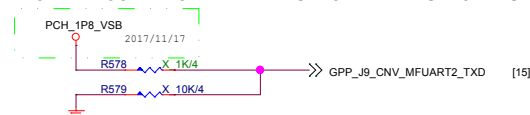
Internal pull-down is disabled after RSMRST# de-assert.

ODT DISABLE



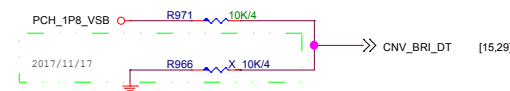
Internal pull-down is disabled after RSMRST# de-assert.

SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE



PCH HAS INTERNAL 20K PD

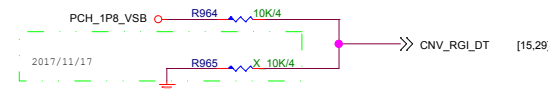
XTAL FREQUENCY SELECTION



XTAL_SEL1 :Internal Pull down

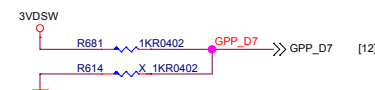
MODEM AND NFC REFERENCE CLOCK SOURCE SELECT

2017/7/12 from Intel's feedback
PU if the integrated CNV1 is enabled
PD if the integrated CNV1 is disabled



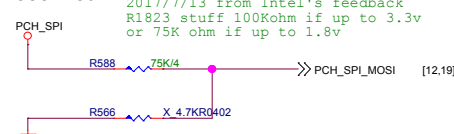
XTAL_SEL2: Internal Pull High.

XTAL INPUT MODE

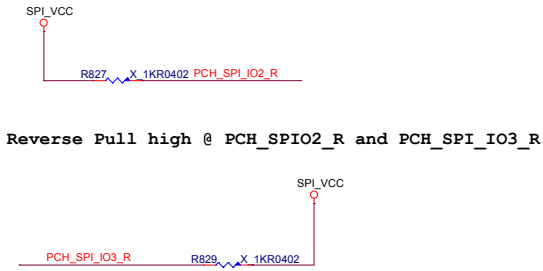


PCH HAS INTERNAL 20K PD

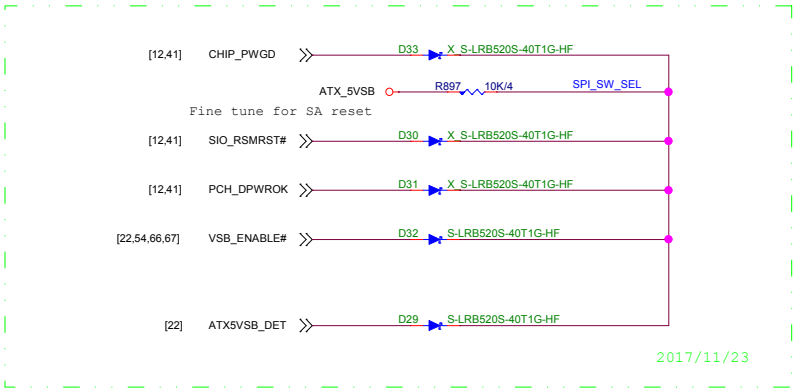
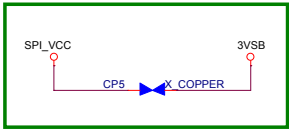
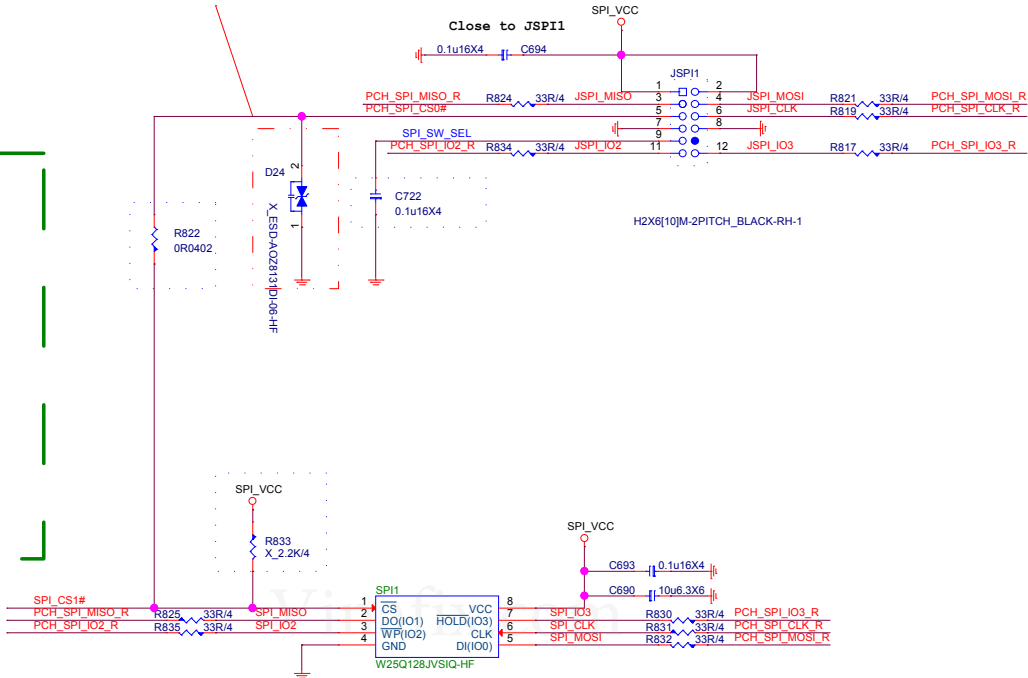
Reserved

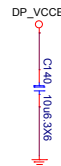
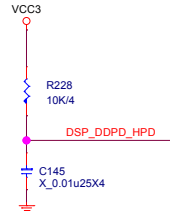
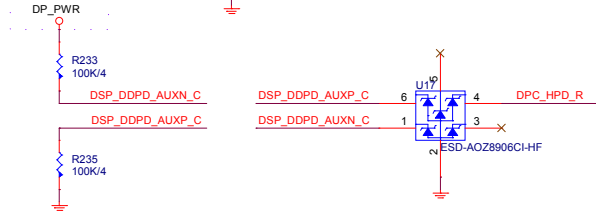
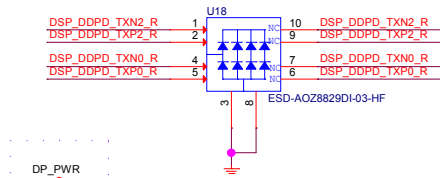
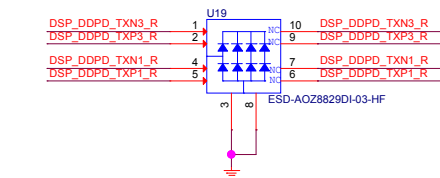


[12] PCH_SPI_CS0# << PCH_SPI_CS0#
[12,18] PCH_SPI_MOSI << PCH_SPI_MOSI R820 0R/4 PCH_SPI_MOSI_R
[12] PCH_SPI_MISO << PCH_SPI_MISO R823 0R/4 PCH_SPI_MISO_R
[12] PCH_SPI_CLK << PCH_SPI_CLK R818 0R/4 PCH_SPI_CLK_R
[12,18] PCH_SPI_IO2 << PCH_SPI_IO2 R826 0R/4 PCH_SPI_IO2_R
[12,18] PCH_SPI_IO3 << PCH_SPI_IO3 R816 0R/4 PCH_SPI_IO3_R

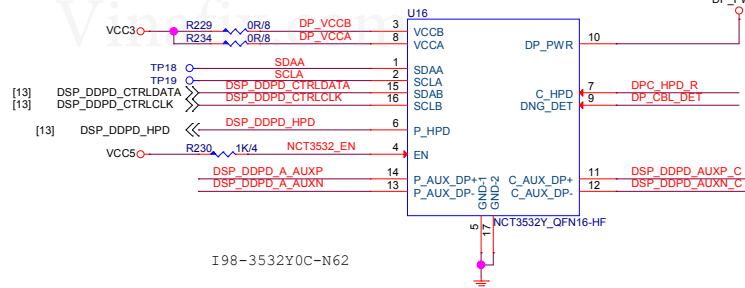


SPI CS# < 25pF
D0G-0402510-SI0

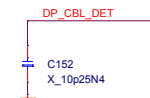
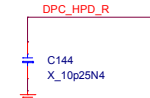
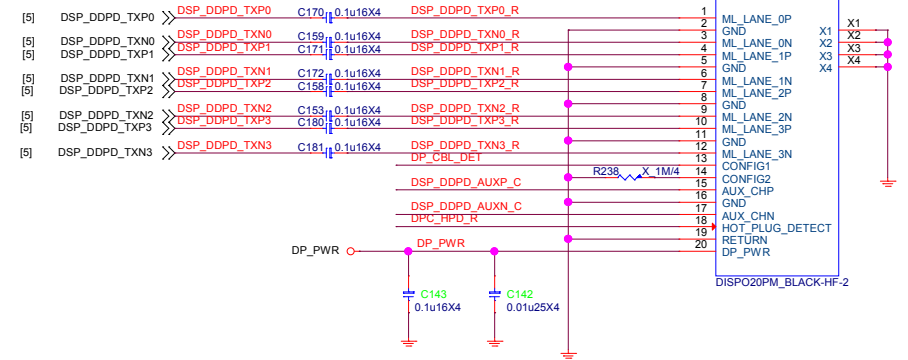




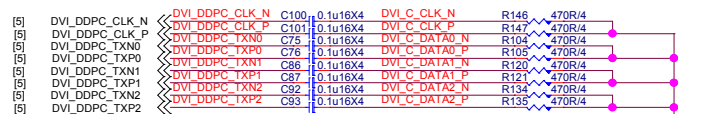
DP_VCCB trace don't less than 30 mil



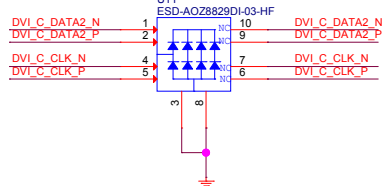
DP



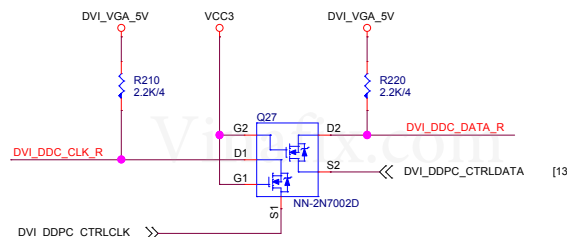
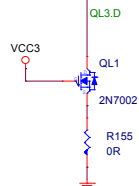
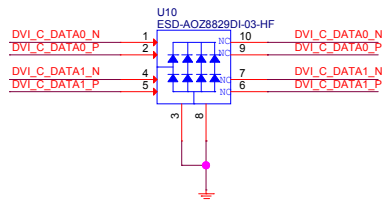
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



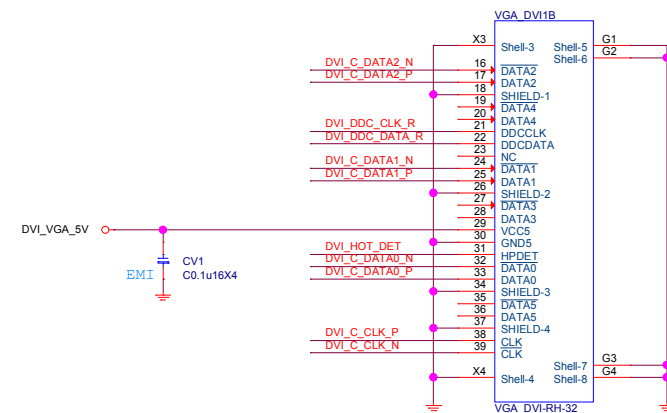
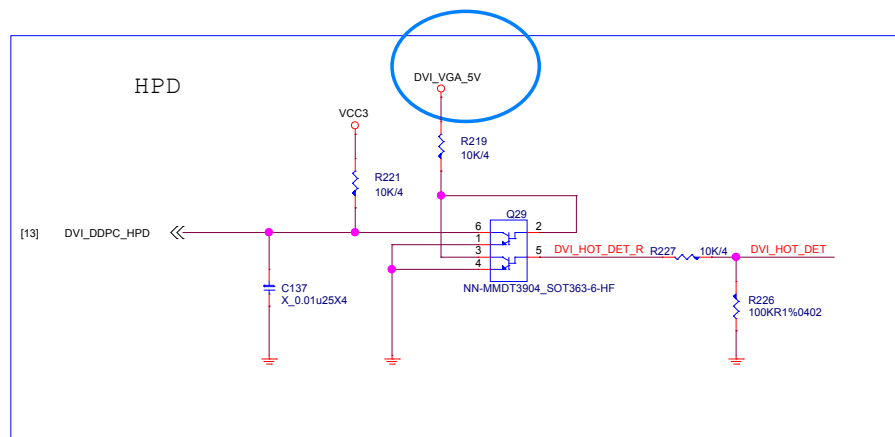
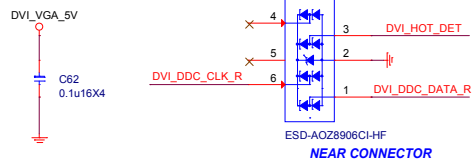
U26 AVL:D0G-05A050C-005
D0G-06A050C-A68



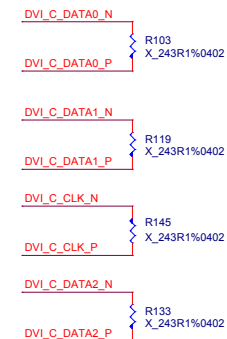
U27 AVL:D0G-05A050C-005
D0G-06A050C-A68



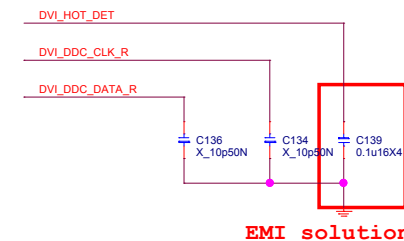
EMI Cap near connector DVI1



For EMI



EMI



msi MICRO-STAR INT'L CO.,LTD.

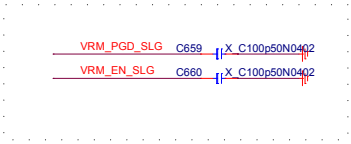
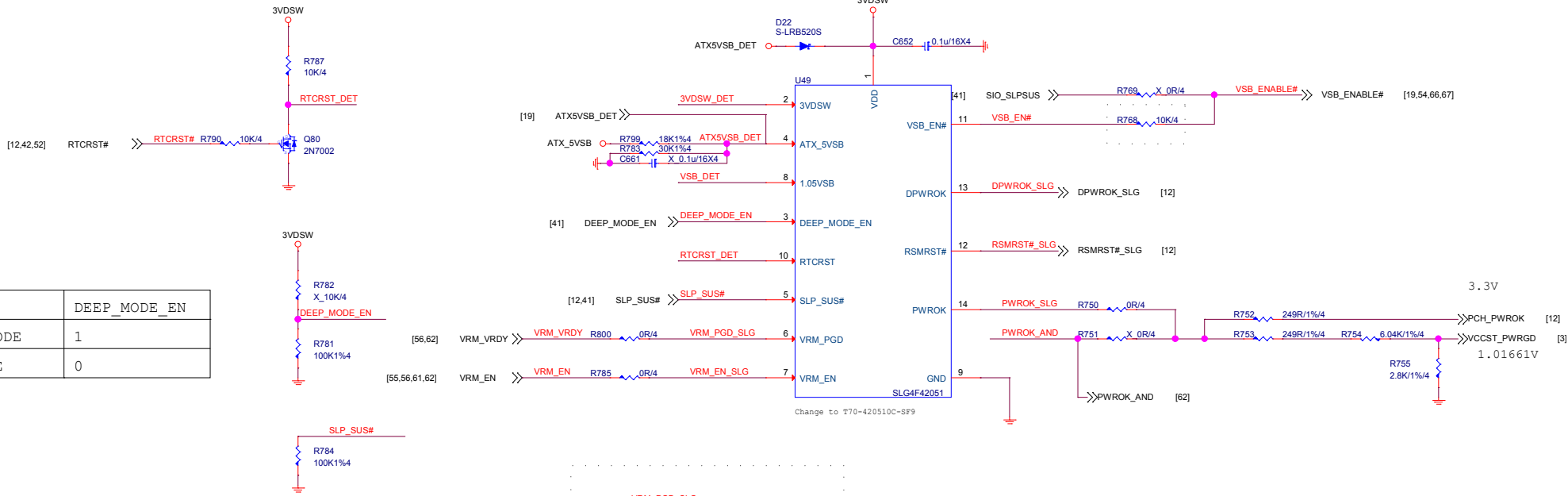
Title DVI Connector

Size Document Number MS-7B98..

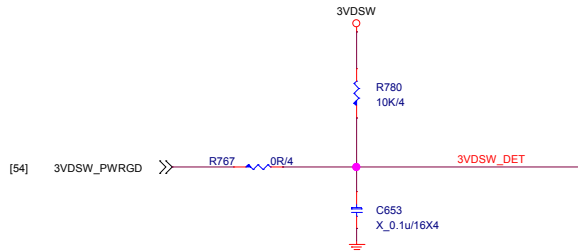
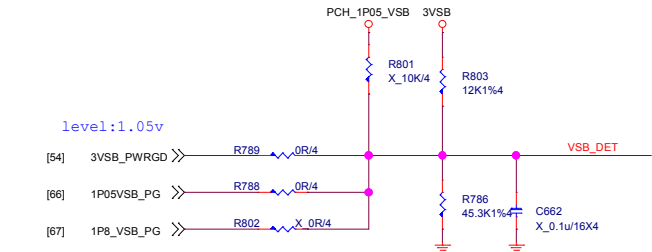
Date Thursday, May 17, 2018 Sheet 21 of 73

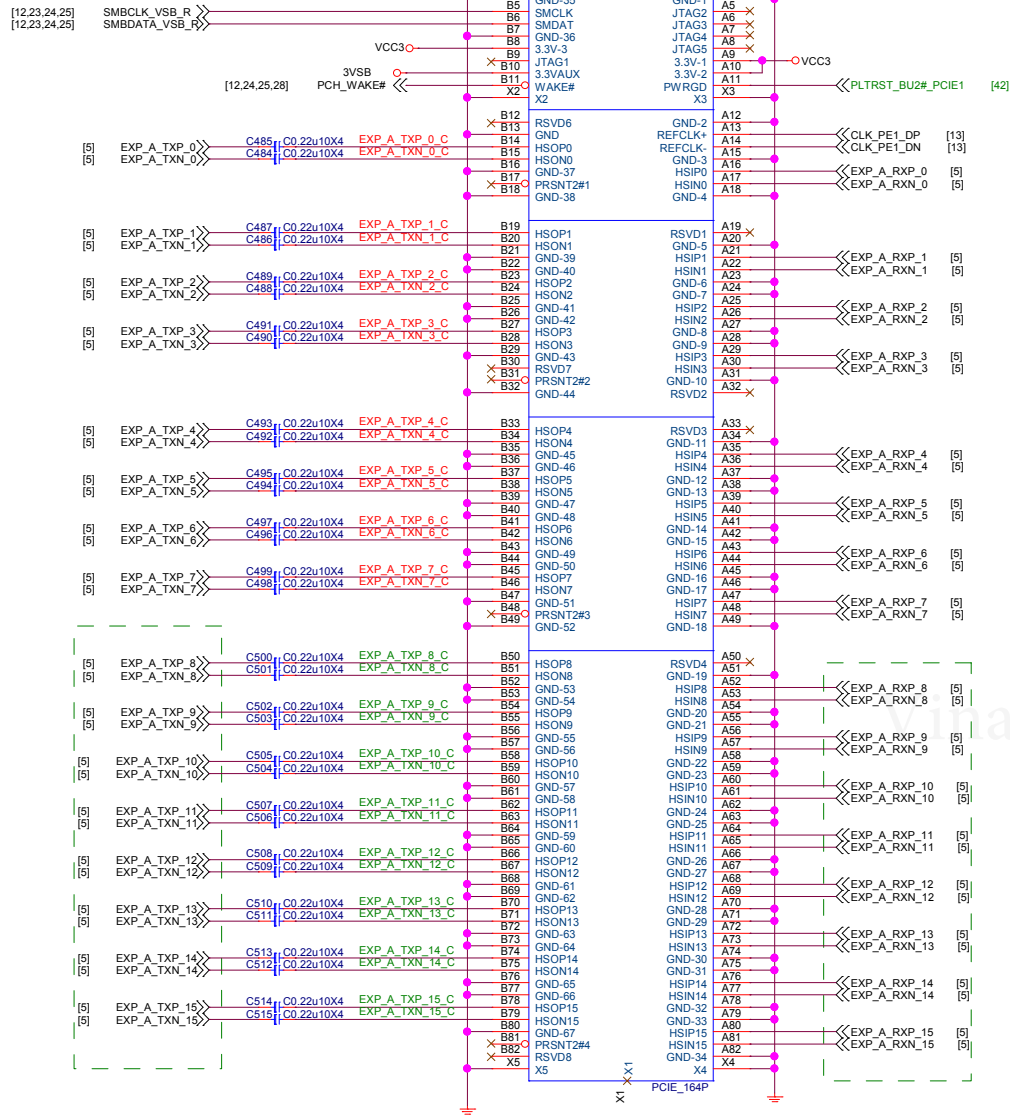
Rev 10

	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

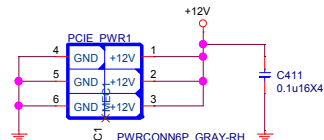
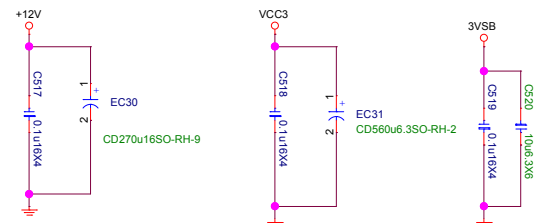
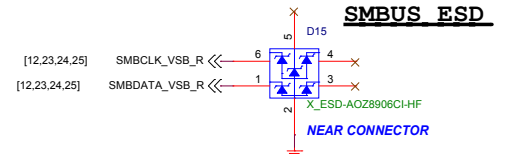


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5.5A at +12V
3A at VCC3
375mA at 3VSB

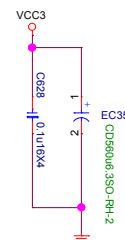
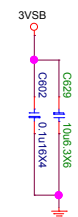
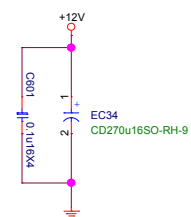
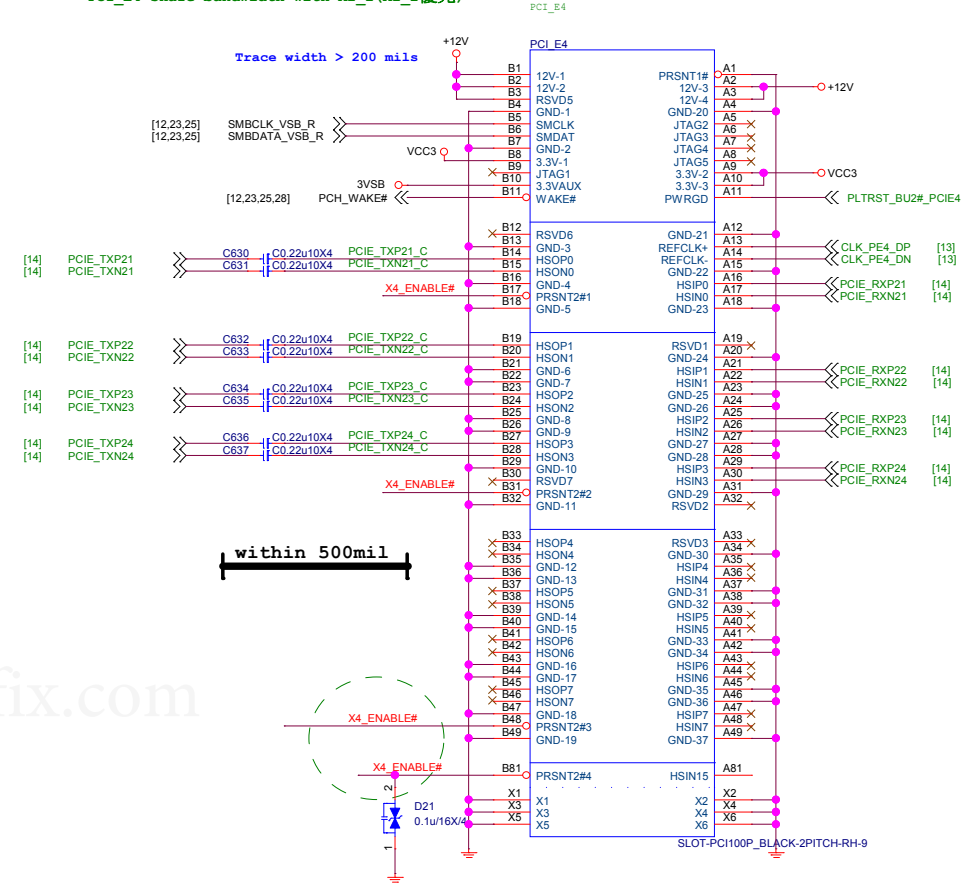


N93-06M0261-H06

PCI Express X4 Slot

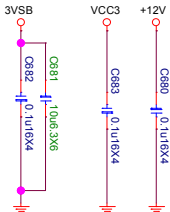
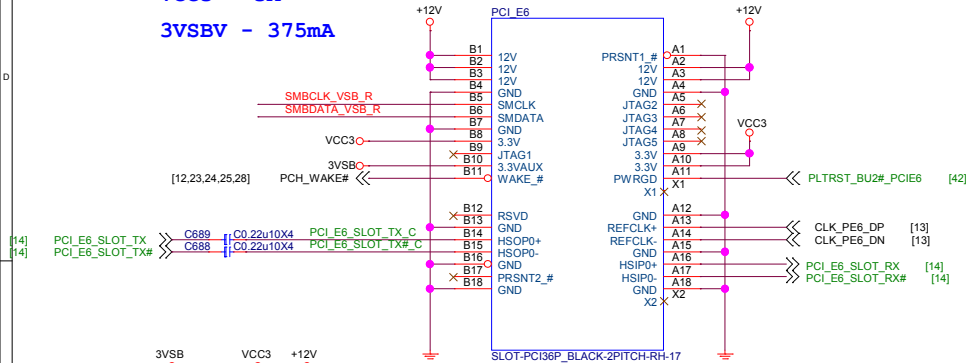
2.1A at +12V
3A at VCC3
375mA at 3VSB

PCI_E4 share bandwidth with M2_2(M2_2優先)

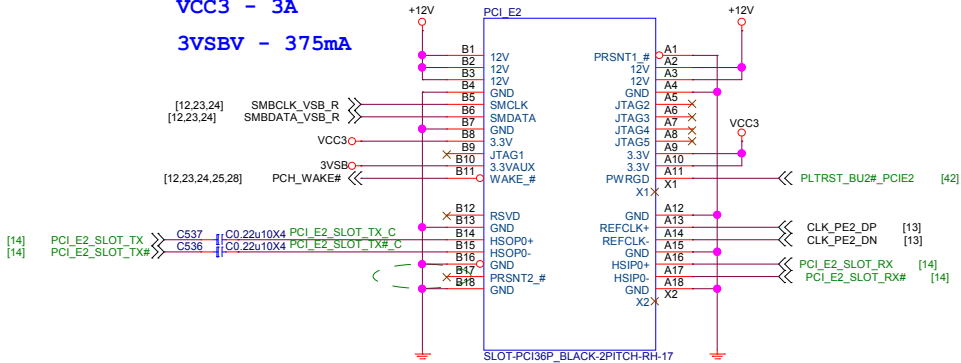


PCH PCIE X1 Slot

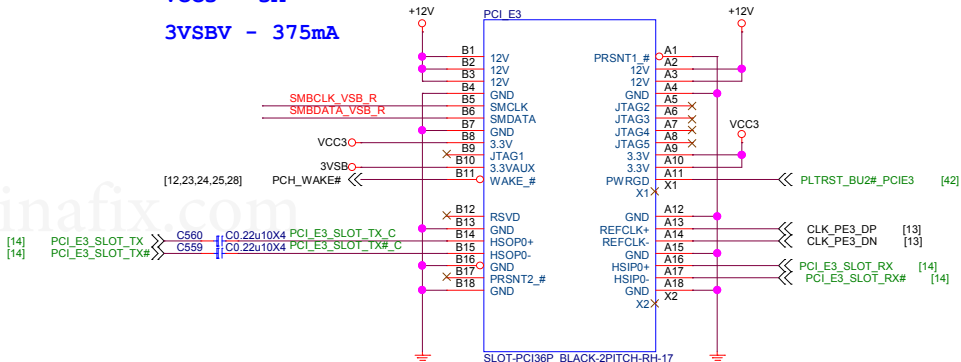
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



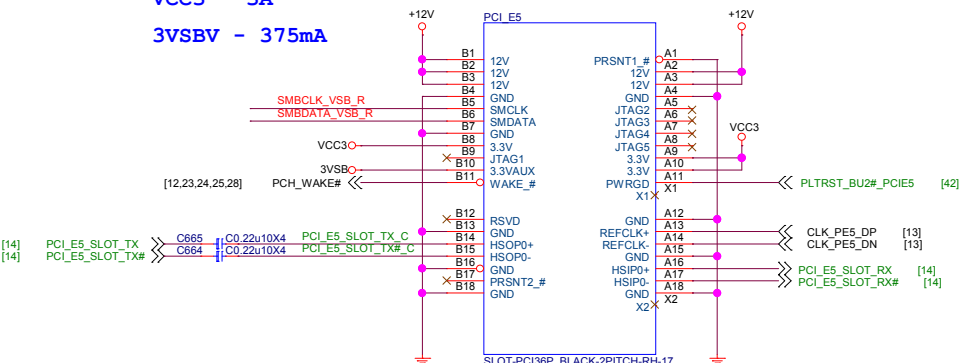
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



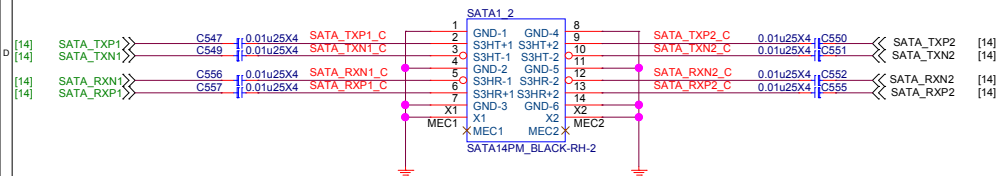
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



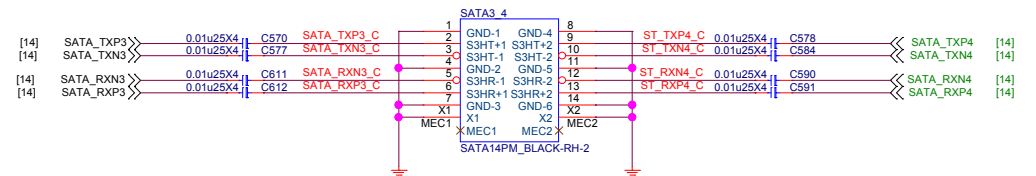
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



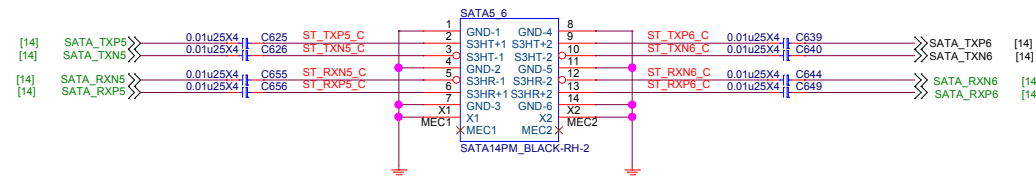
SATA 6G PORT 1.2



SATA 6G PORT 3.4

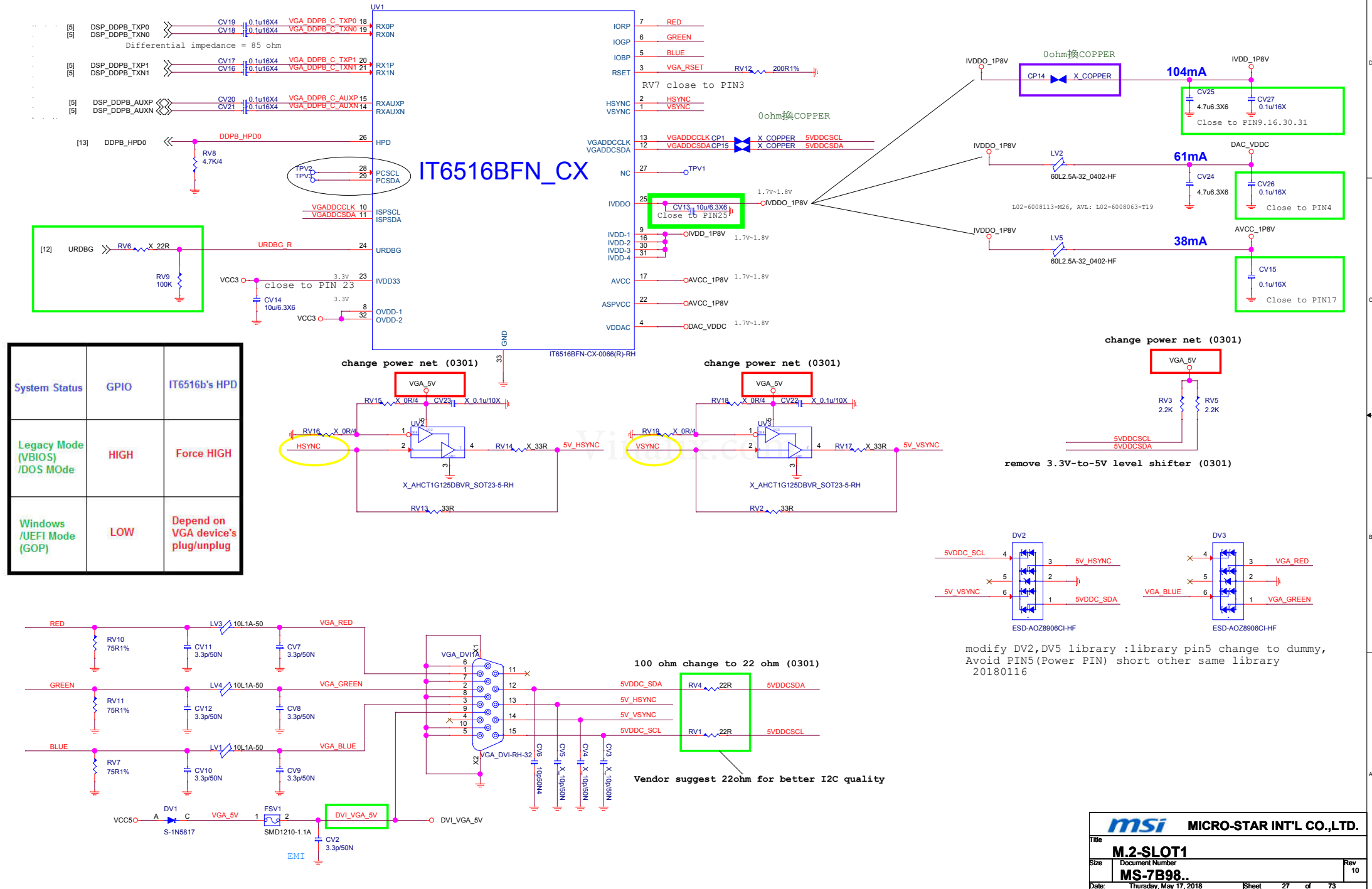


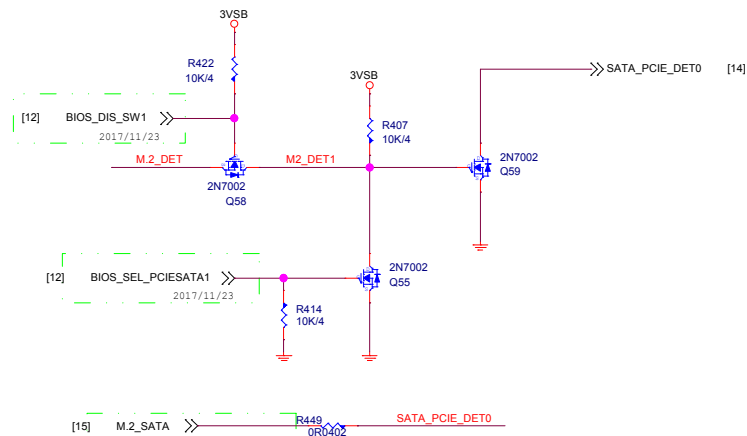
SATA 6G PORT 5.6



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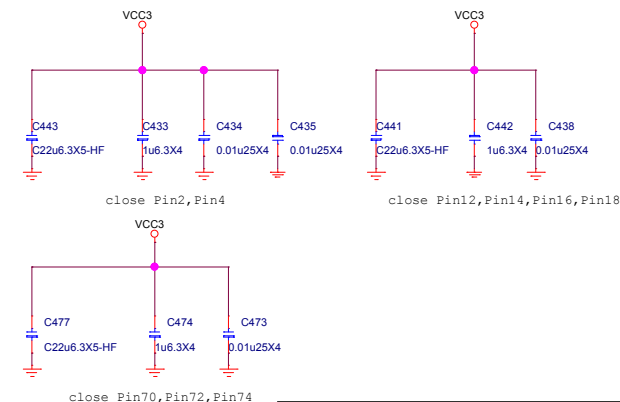
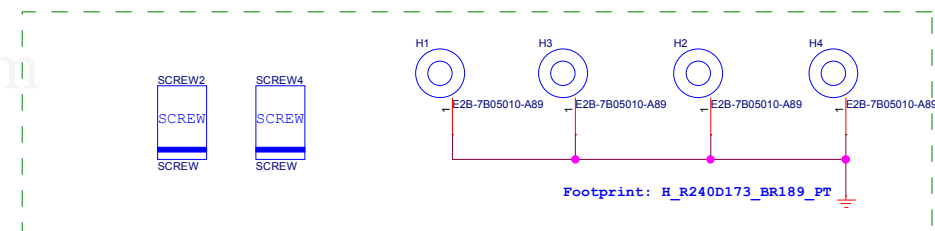
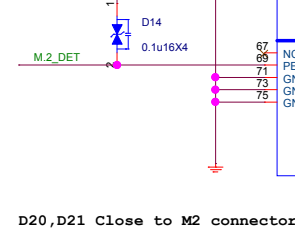
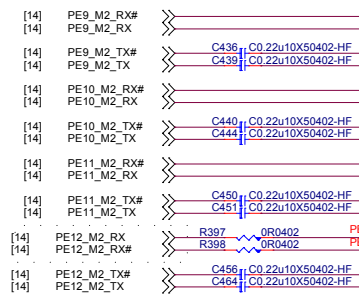
Note:
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

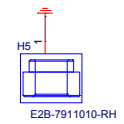
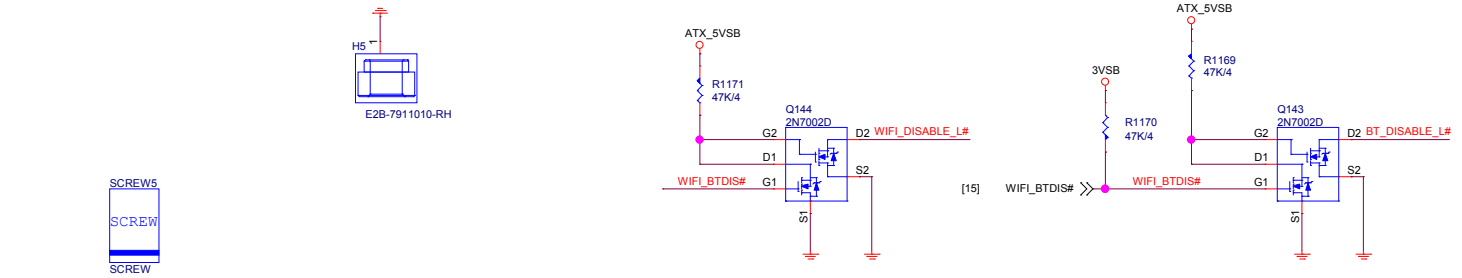
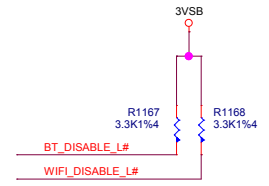
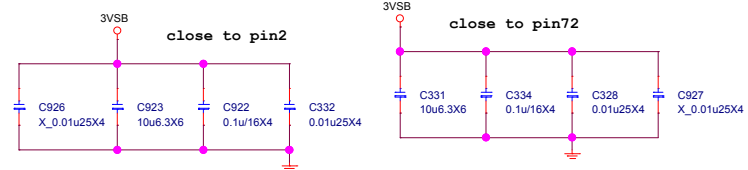
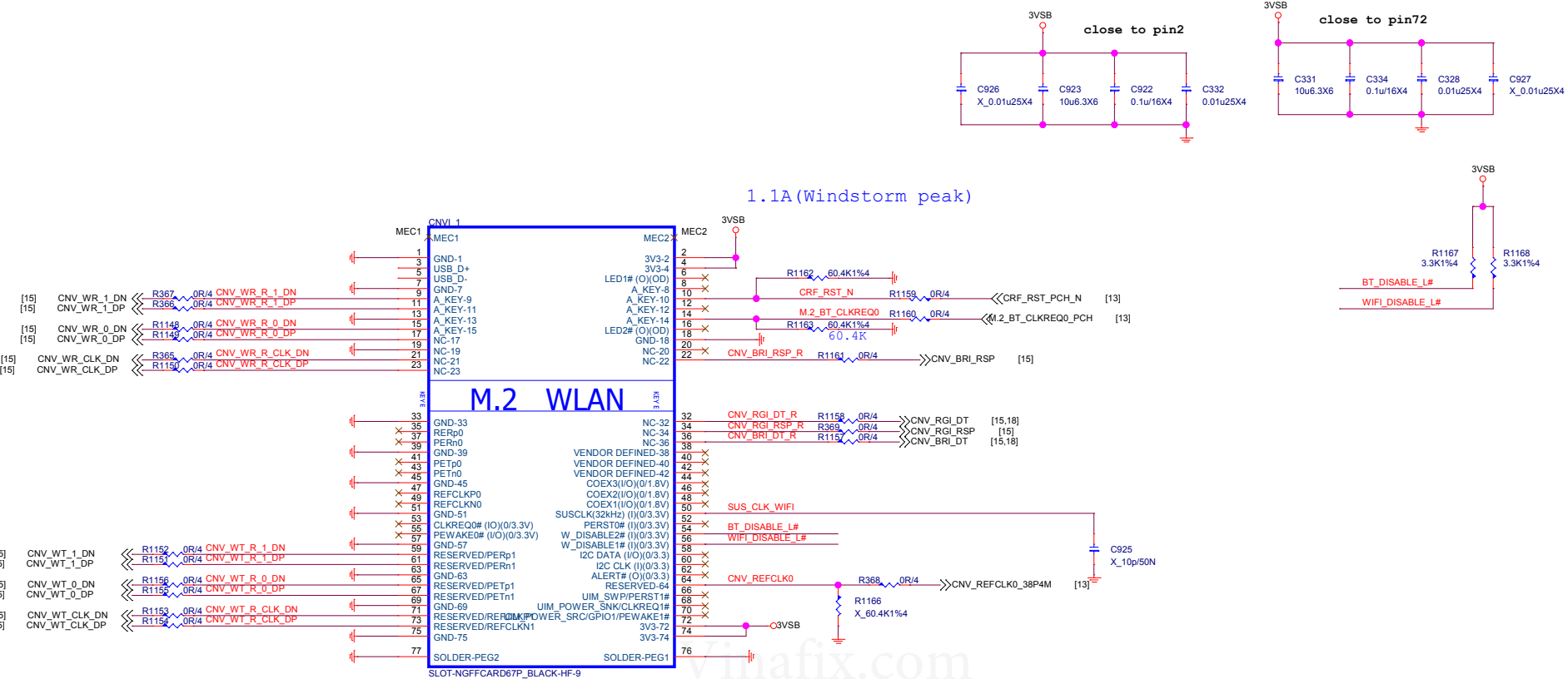




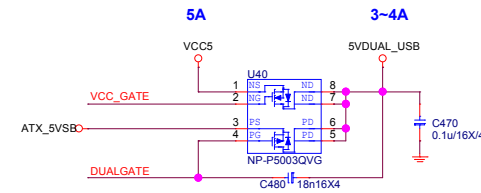
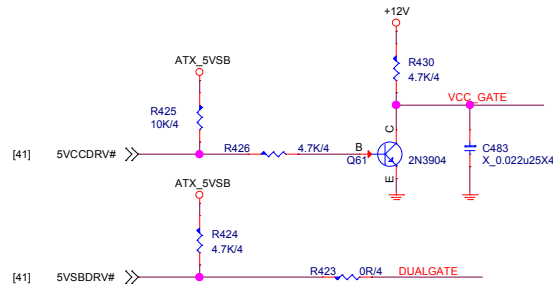
BIOS_MODE

DIS_SW	M1_SEL_PCIESATA	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

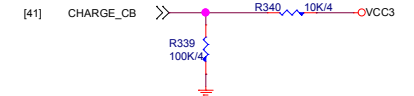




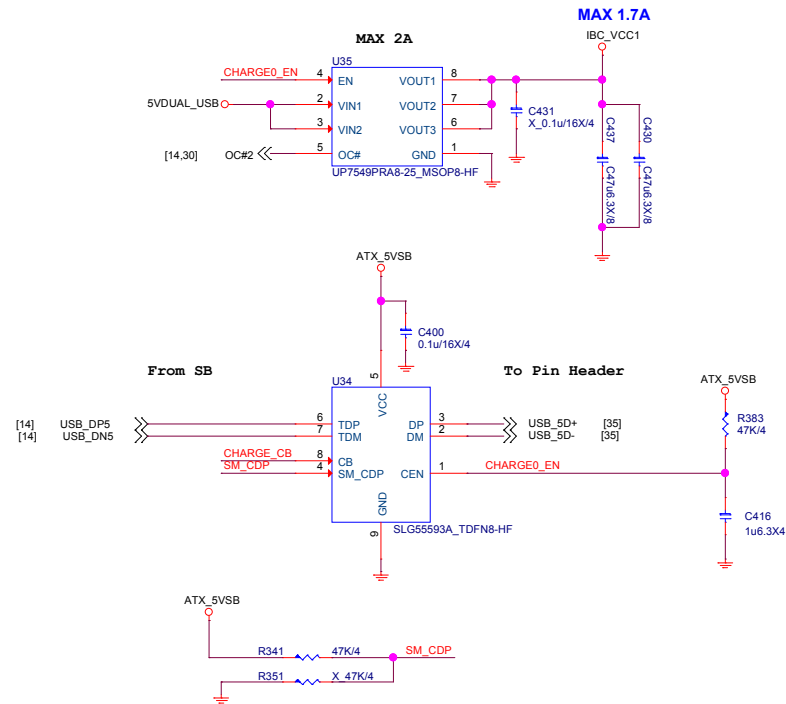
5VDUAL_USB



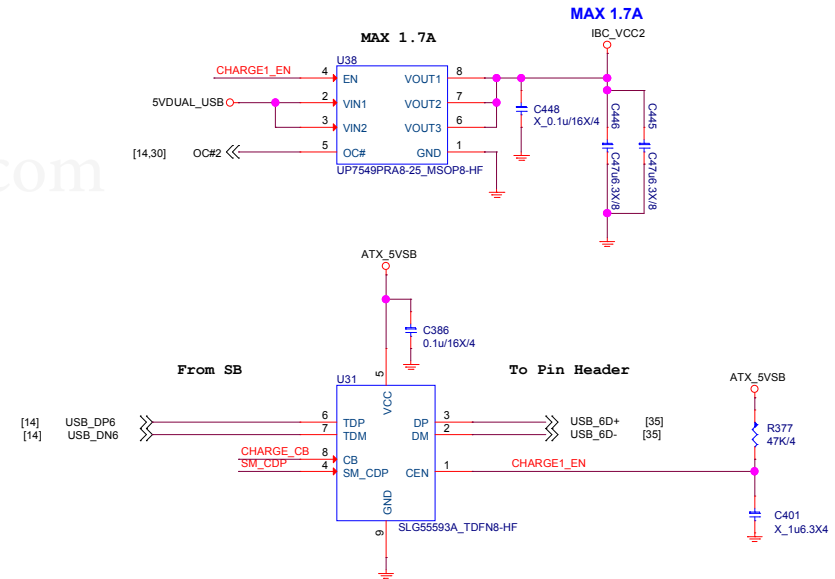
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



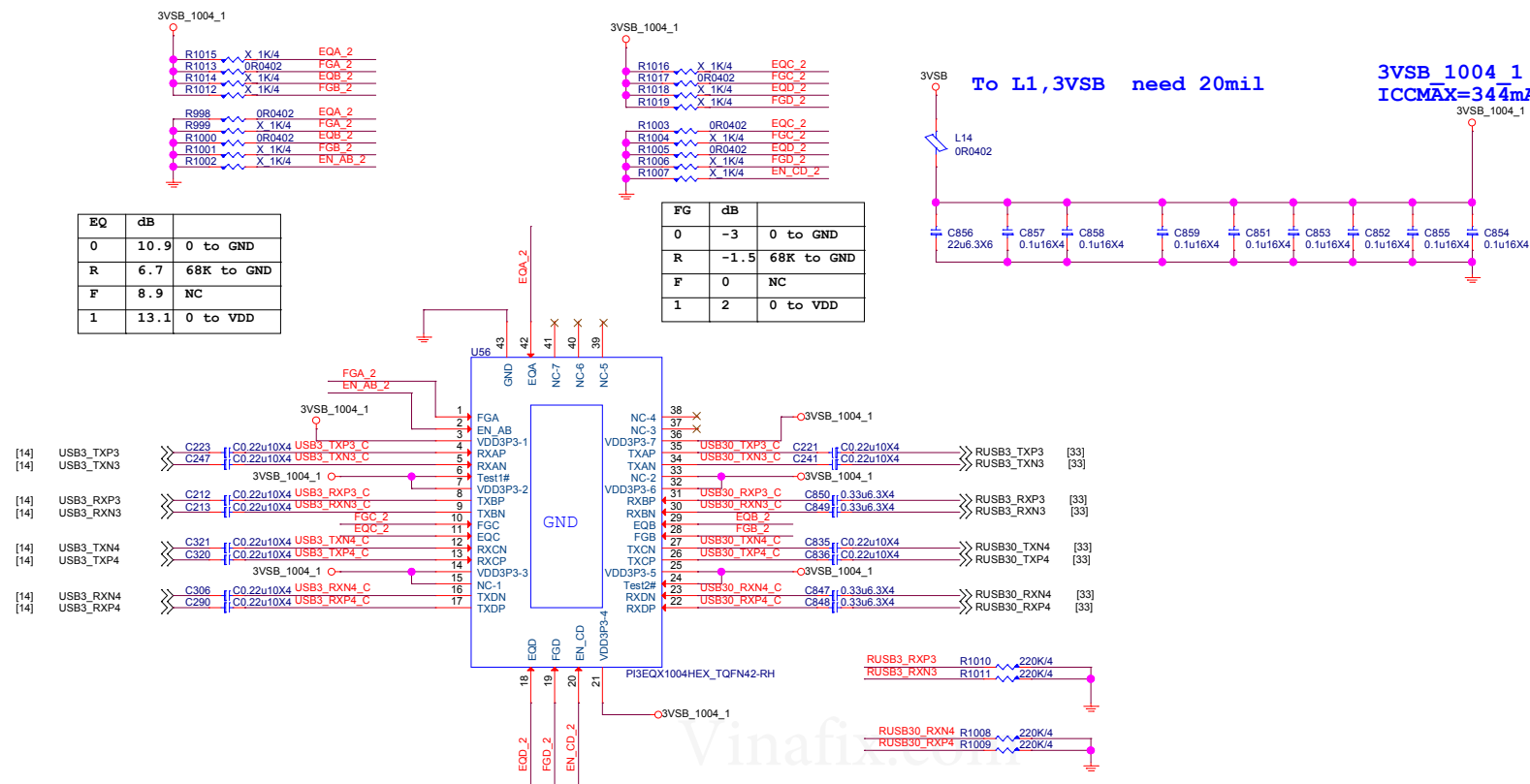
USB POWER PORT 0 For USB Charging

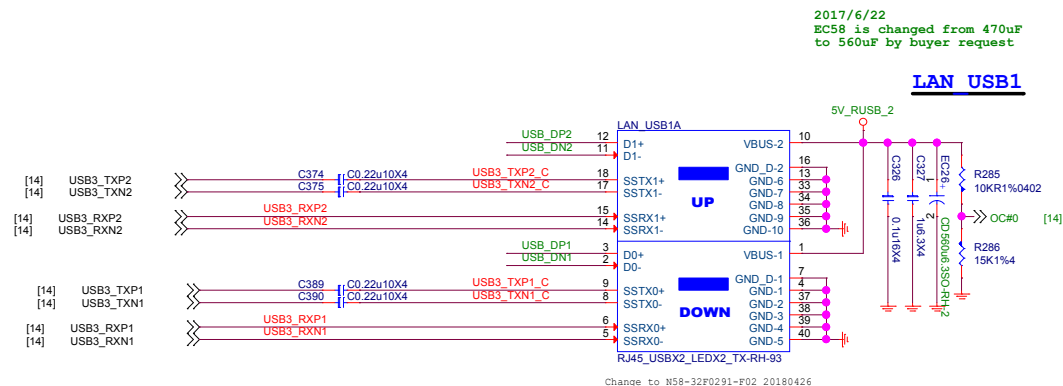
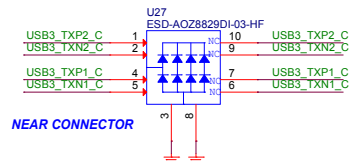
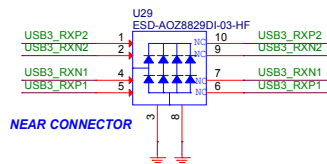
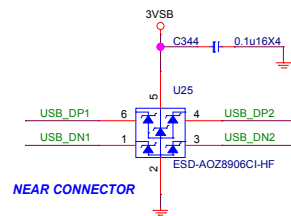


USB POWER PORT 1 For USB Charging

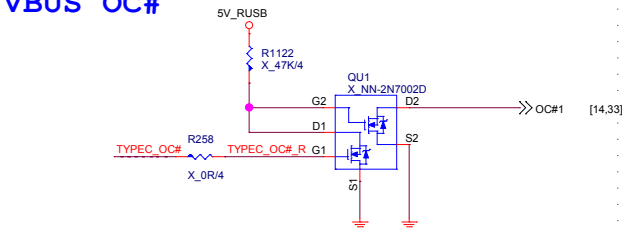


Rear USB3.1 Redriver

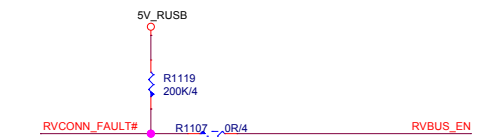




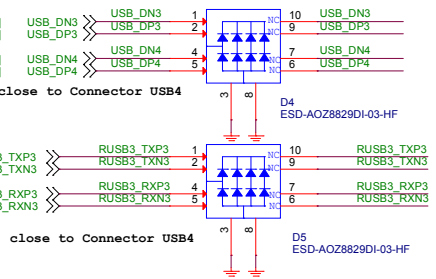
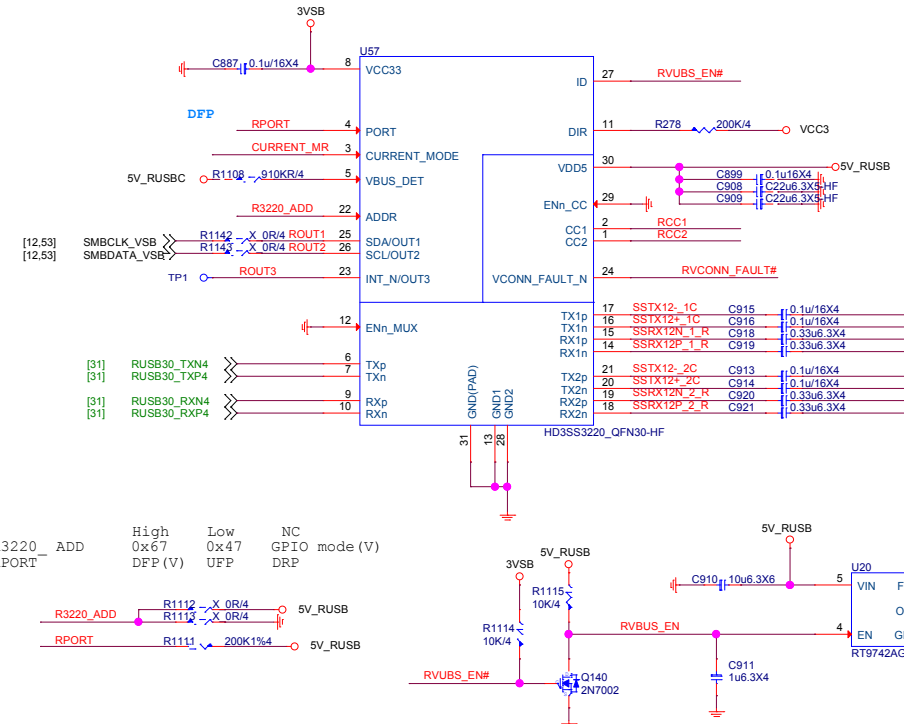
VBUS OC#



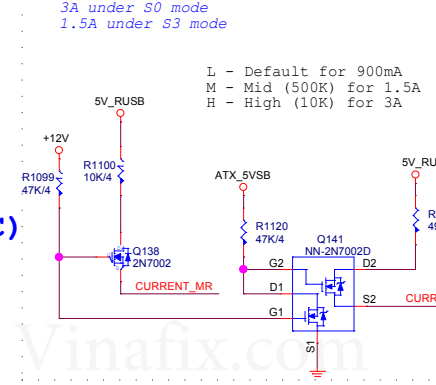
VCONN OC#



USB Type-C MUX with Configuration Channel (CC)

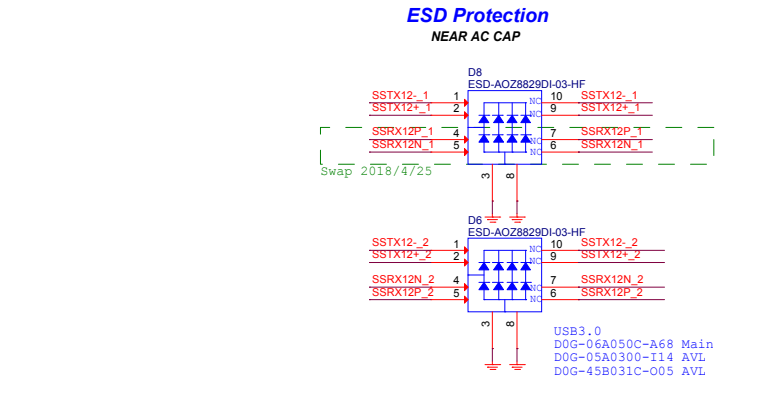
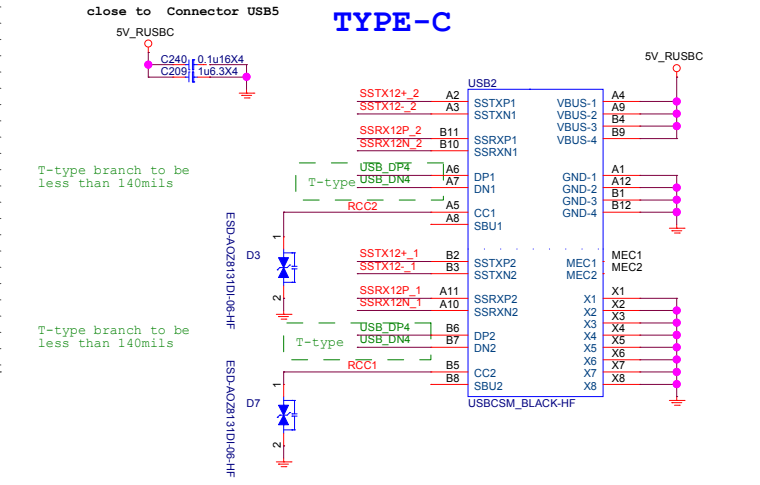
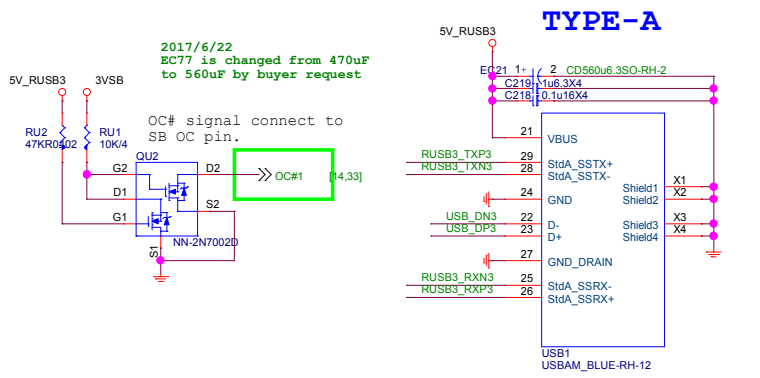


Current Mode



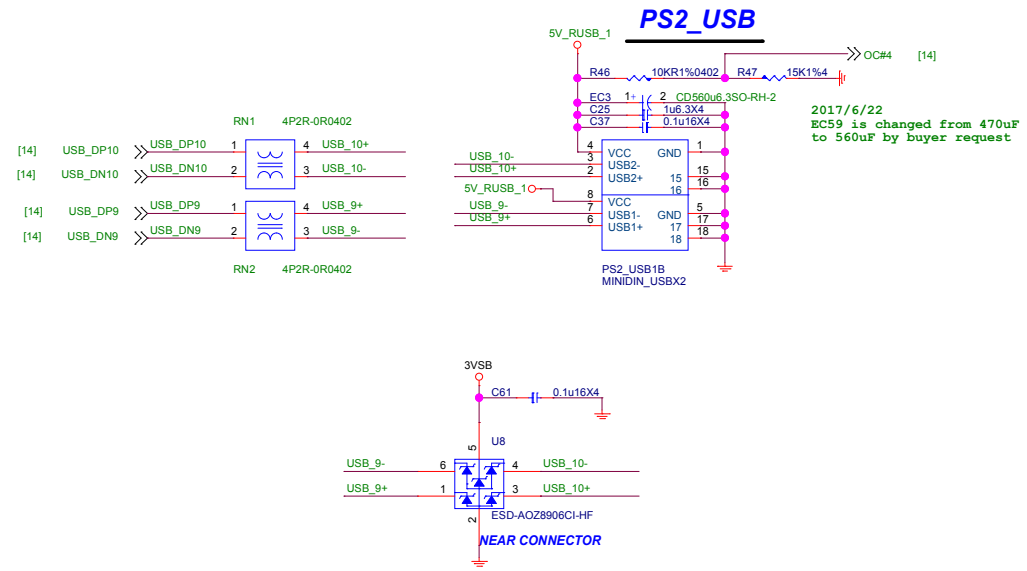
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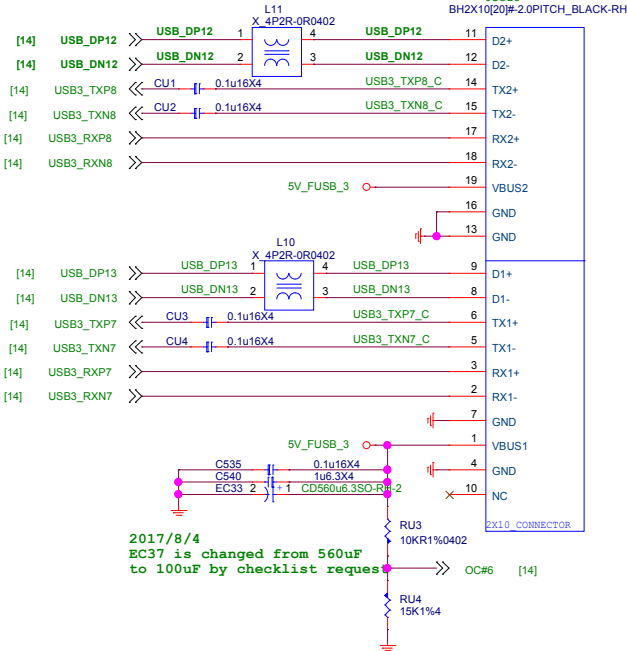
3 A
min 80mil.

REAR USB2.0

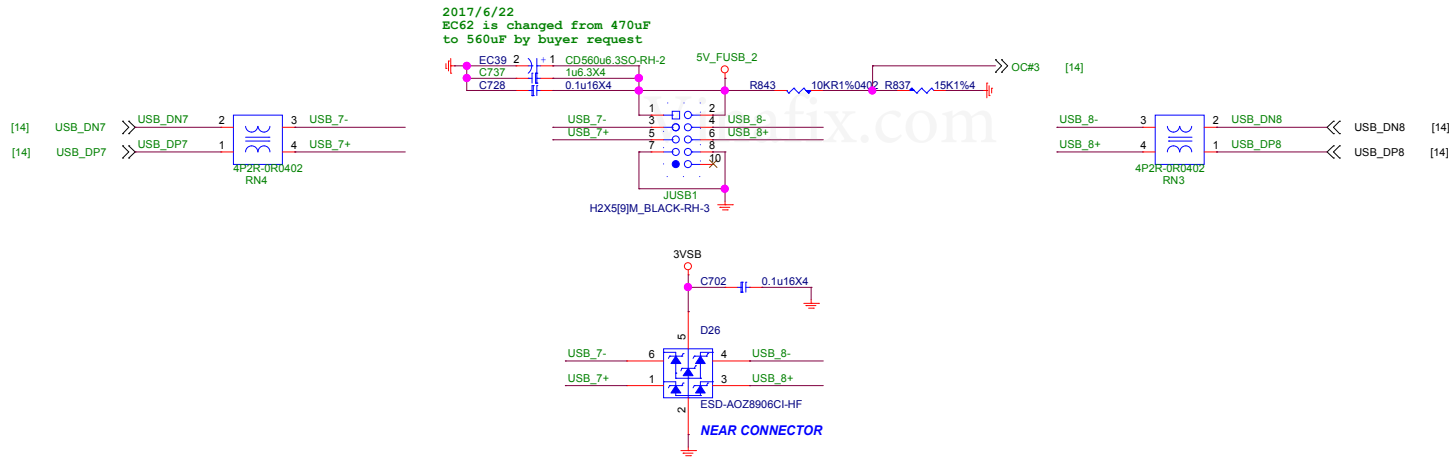
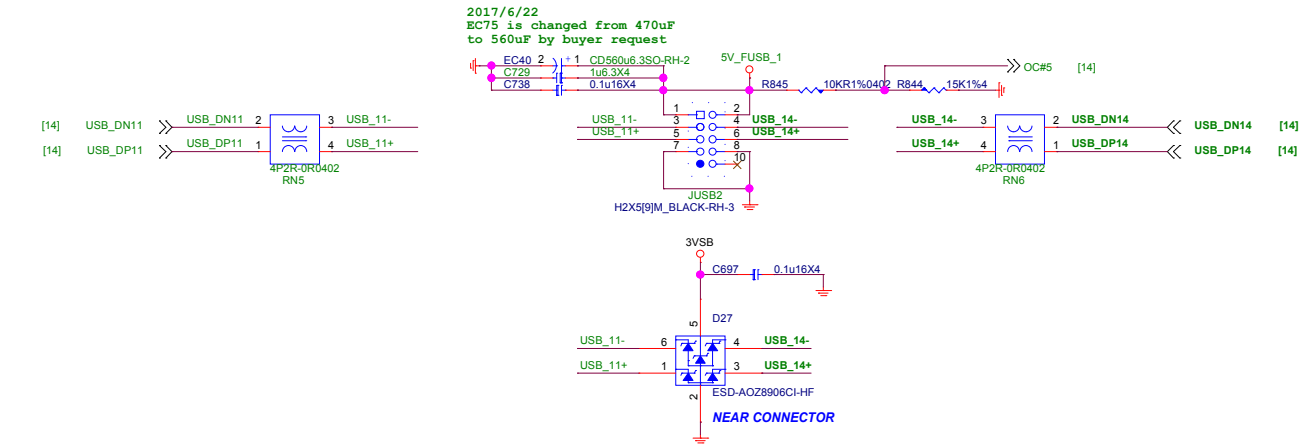


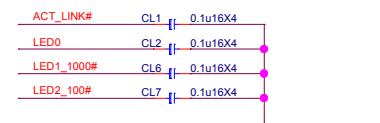
Vinafix.com

B SKU 不上件

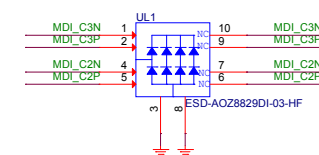


FRONT USB2.0



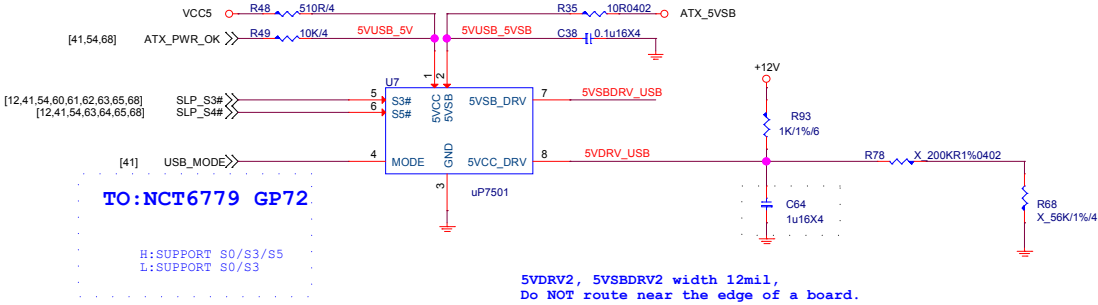


UL2&UL3 close to connector

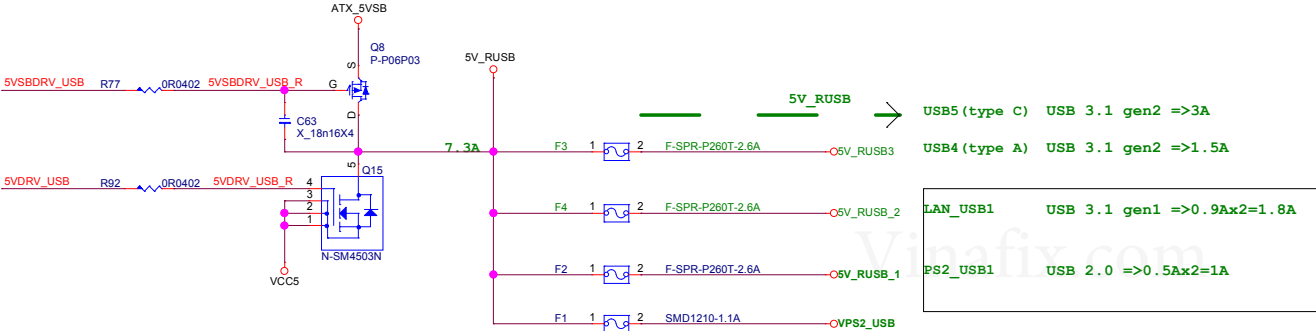


Note: These caps closed to PHY

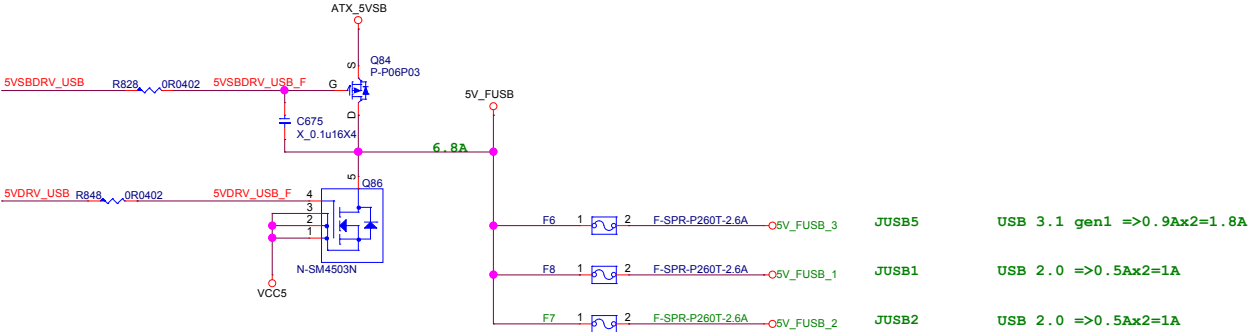
USB POWER



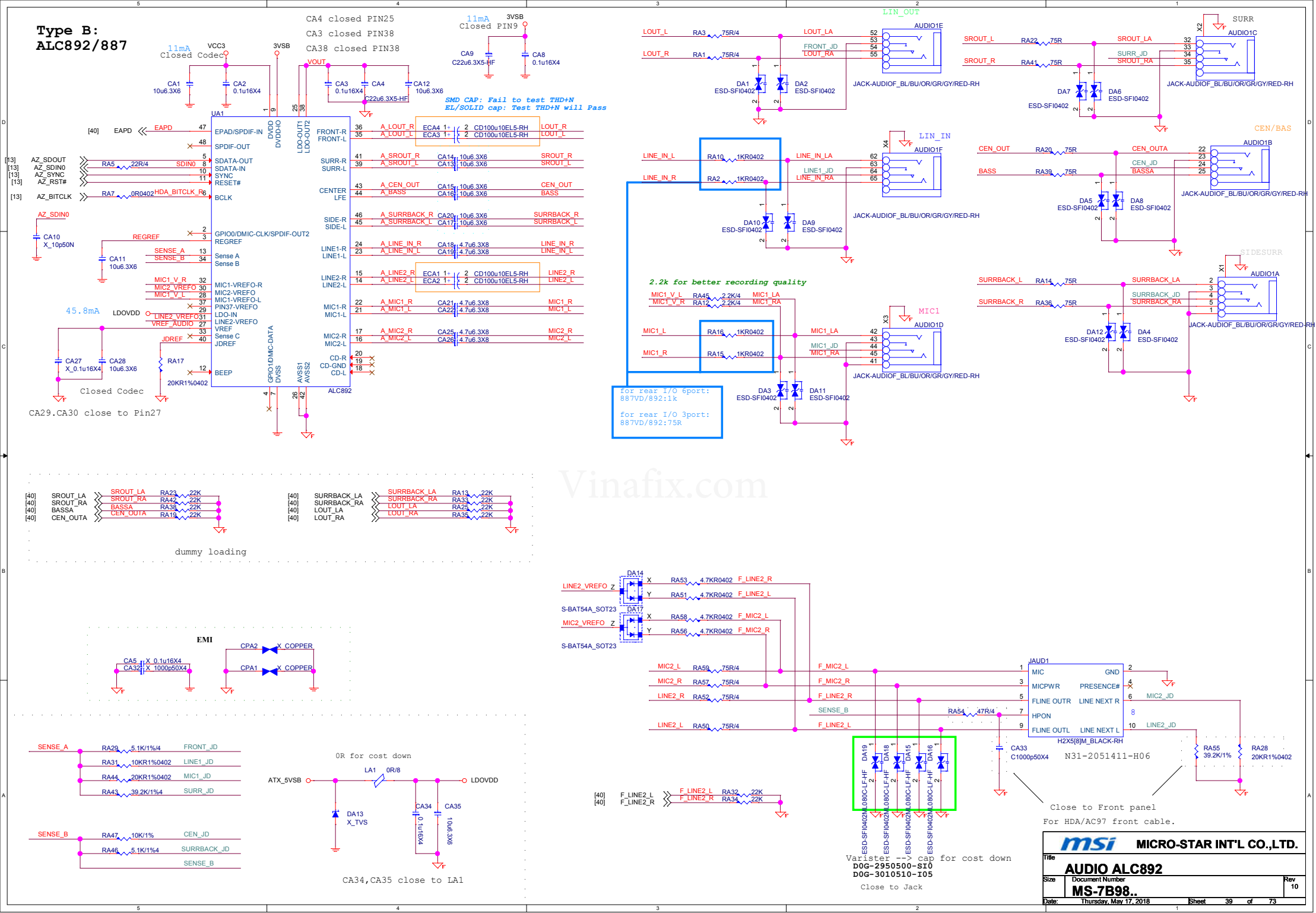
REAR USB PORT POWER



FRONT USB PORT POWER



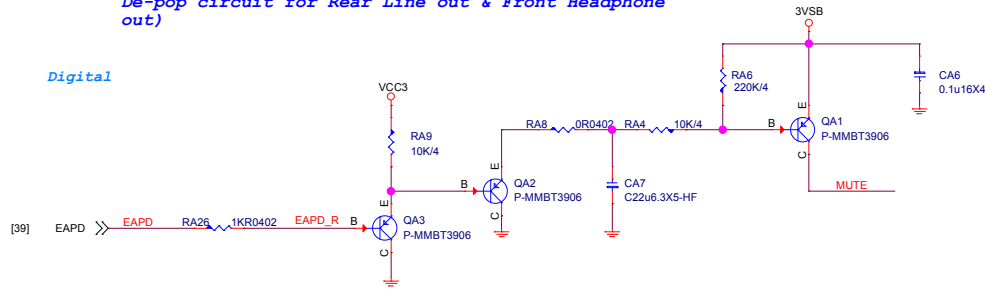
Type B: ALC892/887



Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

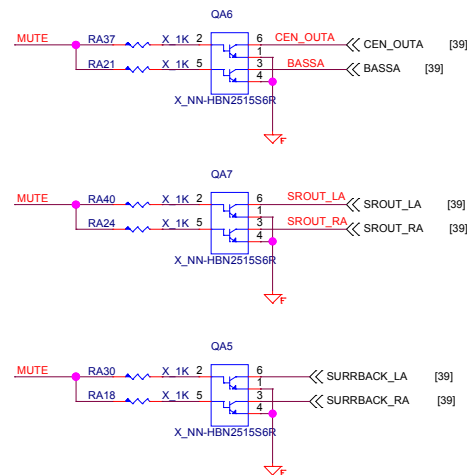
Digital

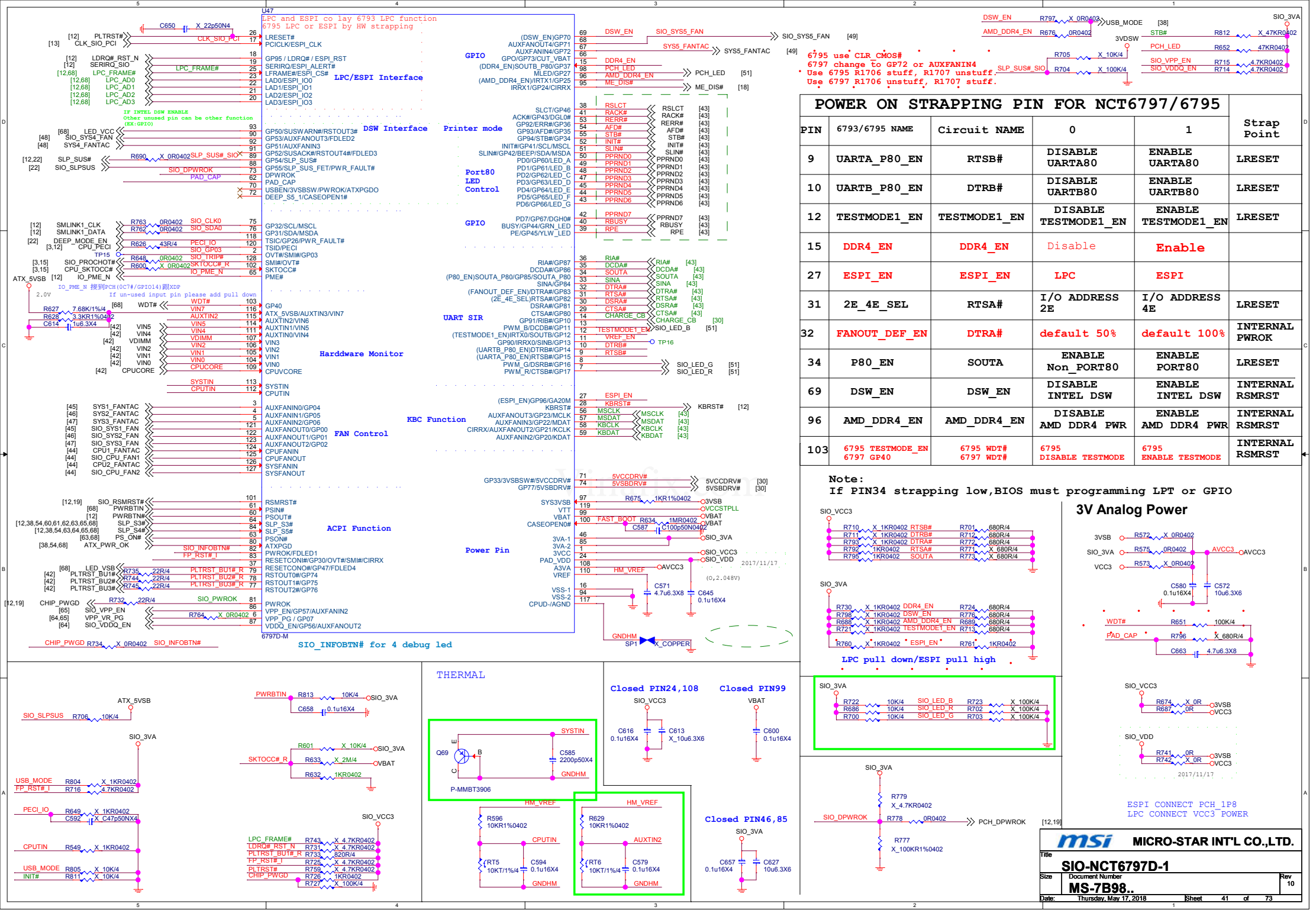


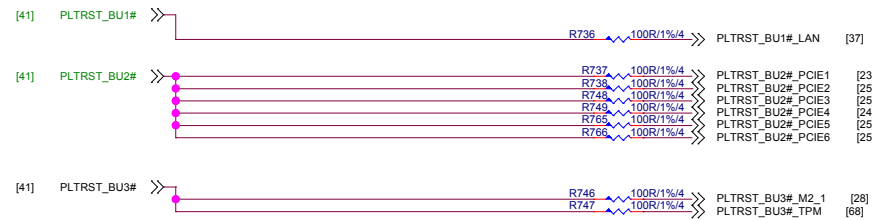
Analog



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA5,CA11, CA12, CA13, CA21, CA22 to TVS)

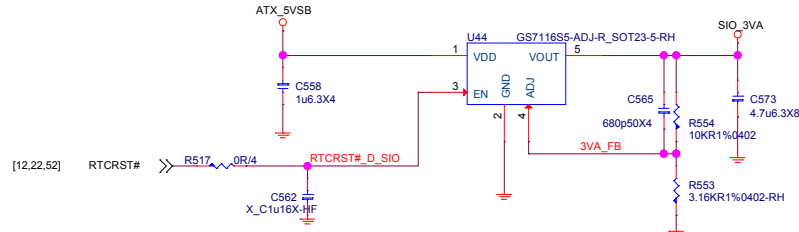
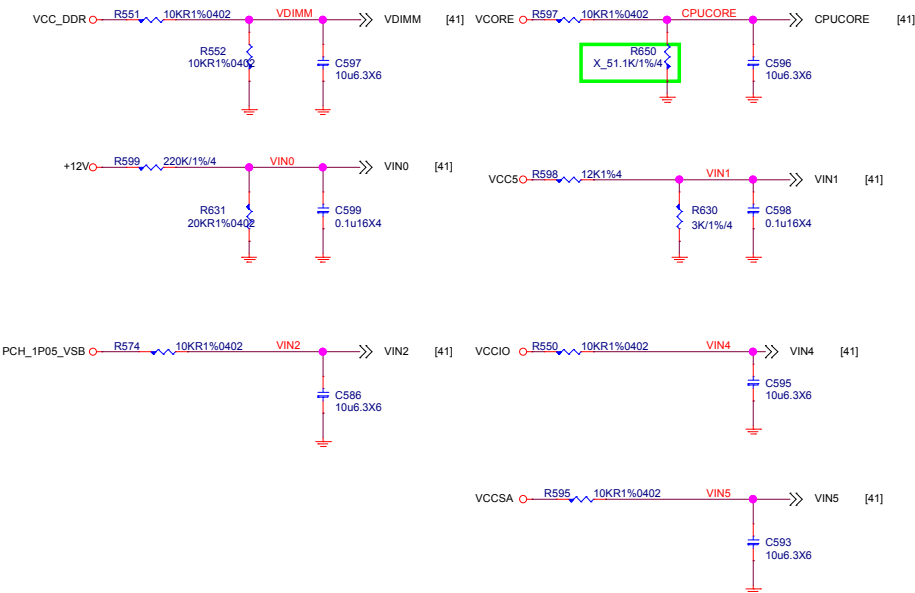




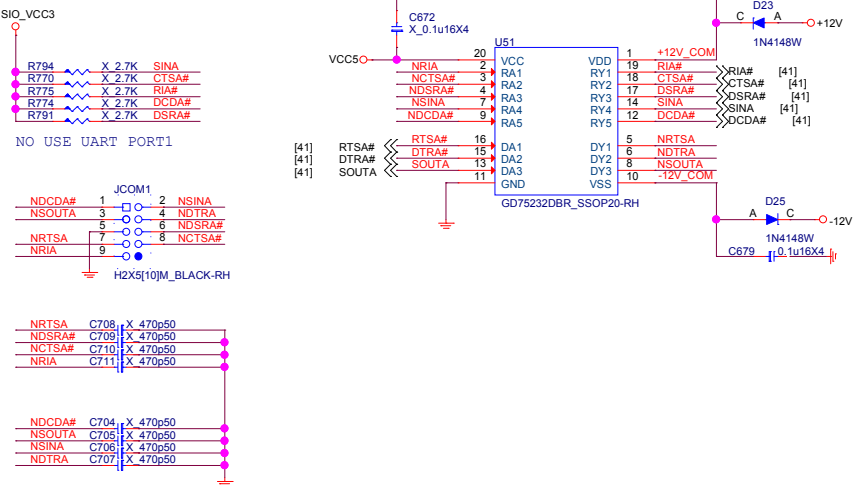


HW Monitor - Voltage

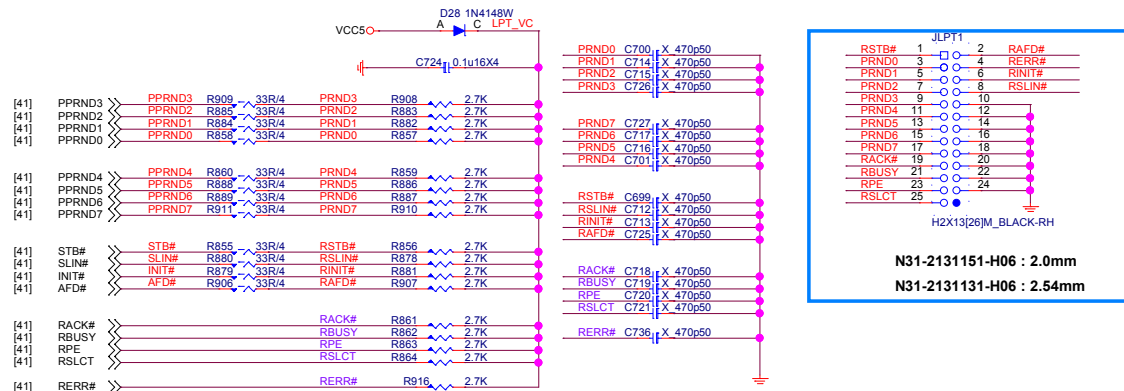
SIO HM Voltage voer 2V will not detect



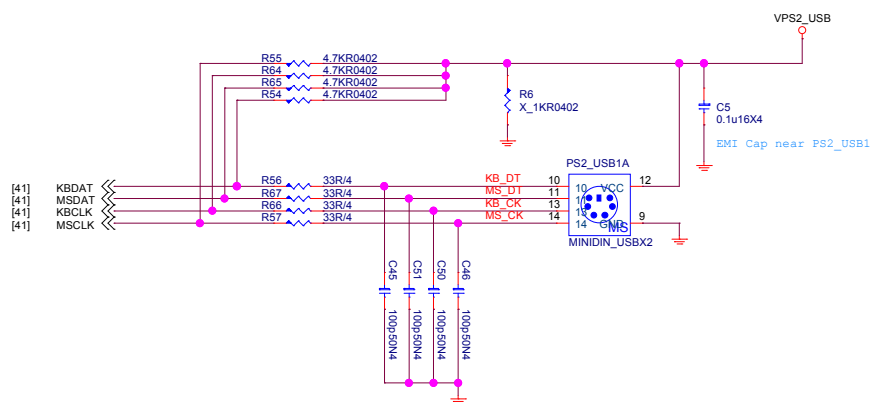
SERIAL PORT 1



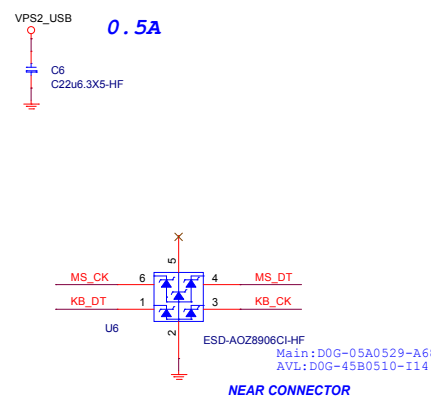
PARALLAL PORT



PS2 KEYBOARD & MOUSE CONNECTOR

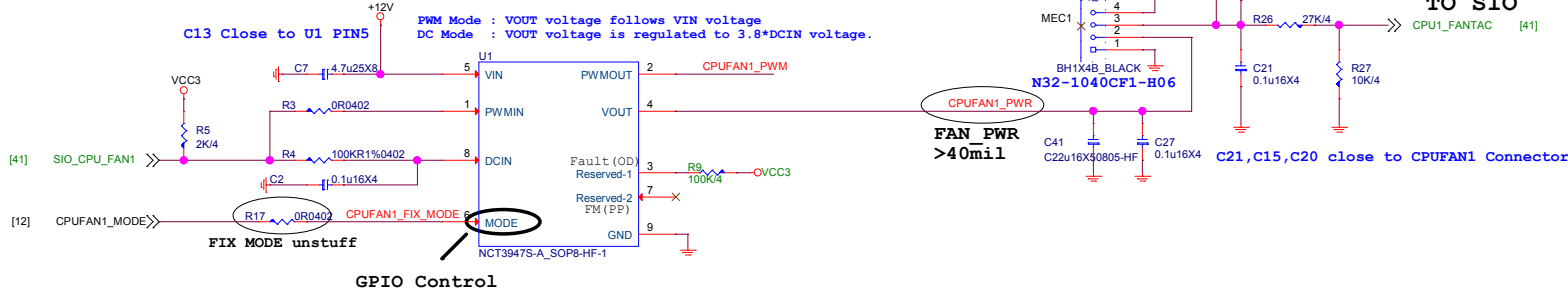


PS2 Power



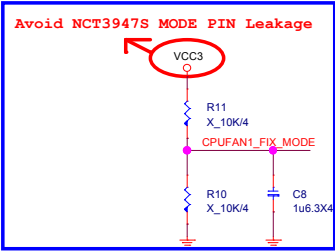
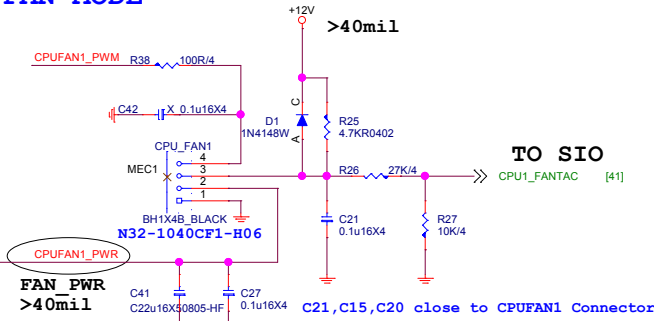
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

- 1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
- 2. GPIO可以由BIOS切換 PWM/DC MODE
- 3. OCF拉回GPIO給BIOS認
- 4. PWM OR DC FAN拉回GPIO給BIOS認
- 5. FAN轉速加快的時候由SOFTWARE 控制GPIO讓燈的變化



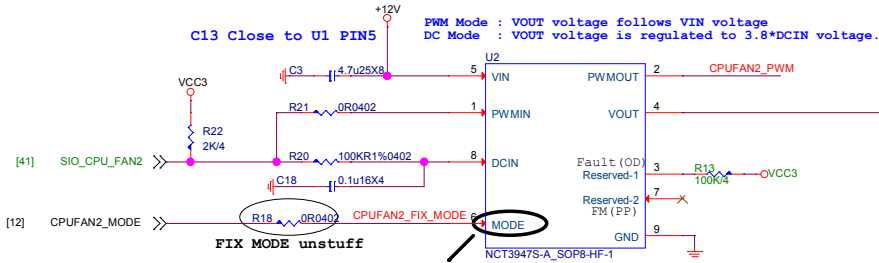
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



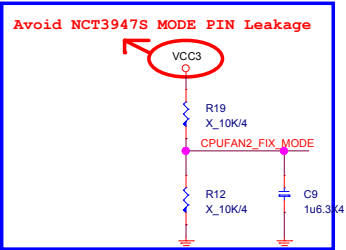
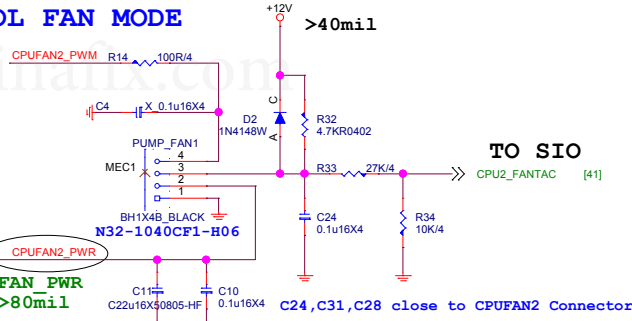
Resever For FIX DC or PWM MODE USE By PM SPEC

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

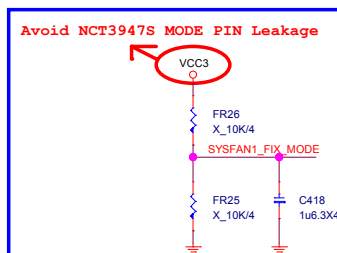
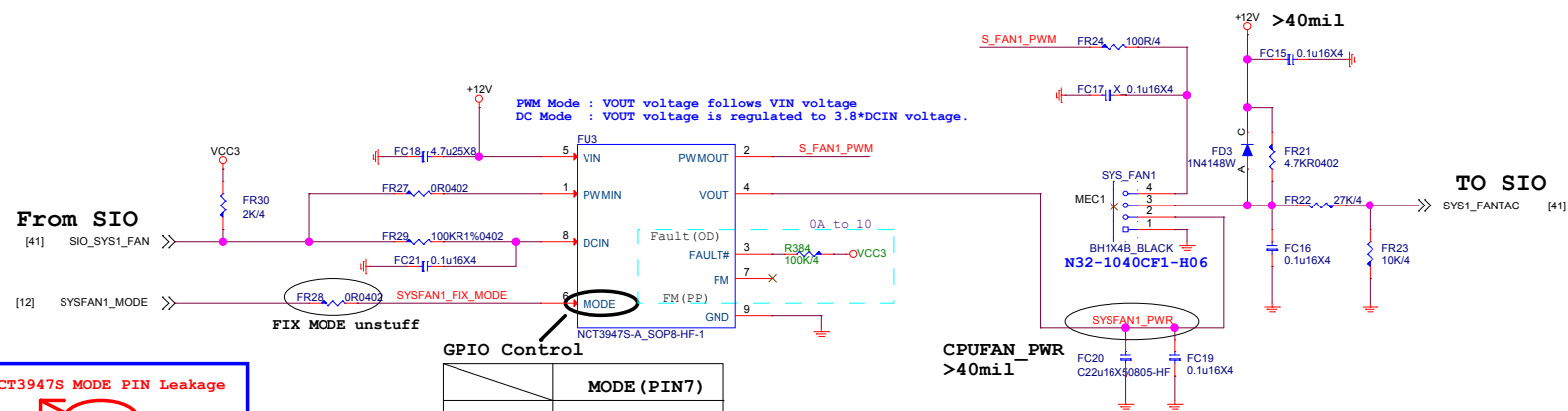
Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

- 1. MODE : USE MODE PIN change FAN MODE (PWM or DC FAN)
- 2. FAULT : USE FAULT PIN Triger OVT/OCF Protection, LOW Atcive (Reserve NEW IC)
- 3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information (Reserve NEW IC)

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



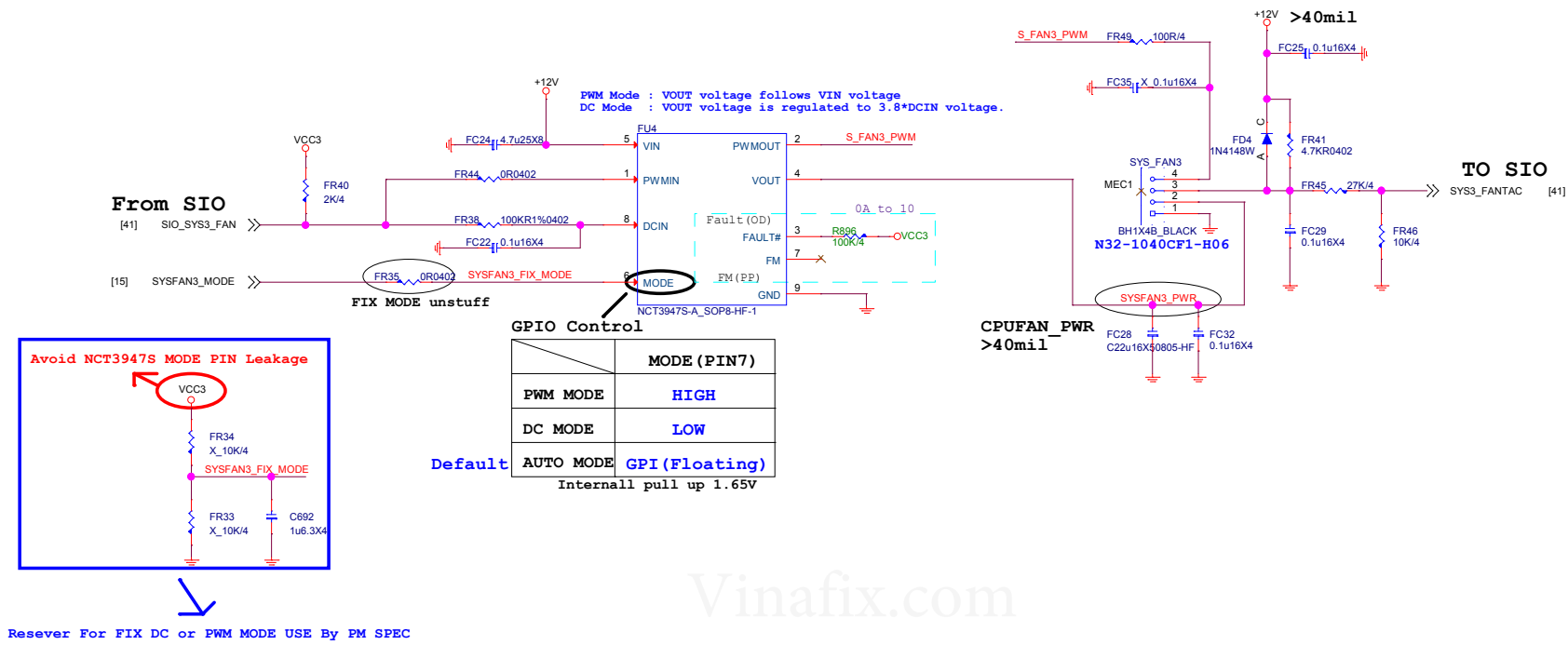
Resever For FIX DC or PWM MODE USE By PM SPEC

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Internal pull up 1.65V

Internall pull up 1.65V

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



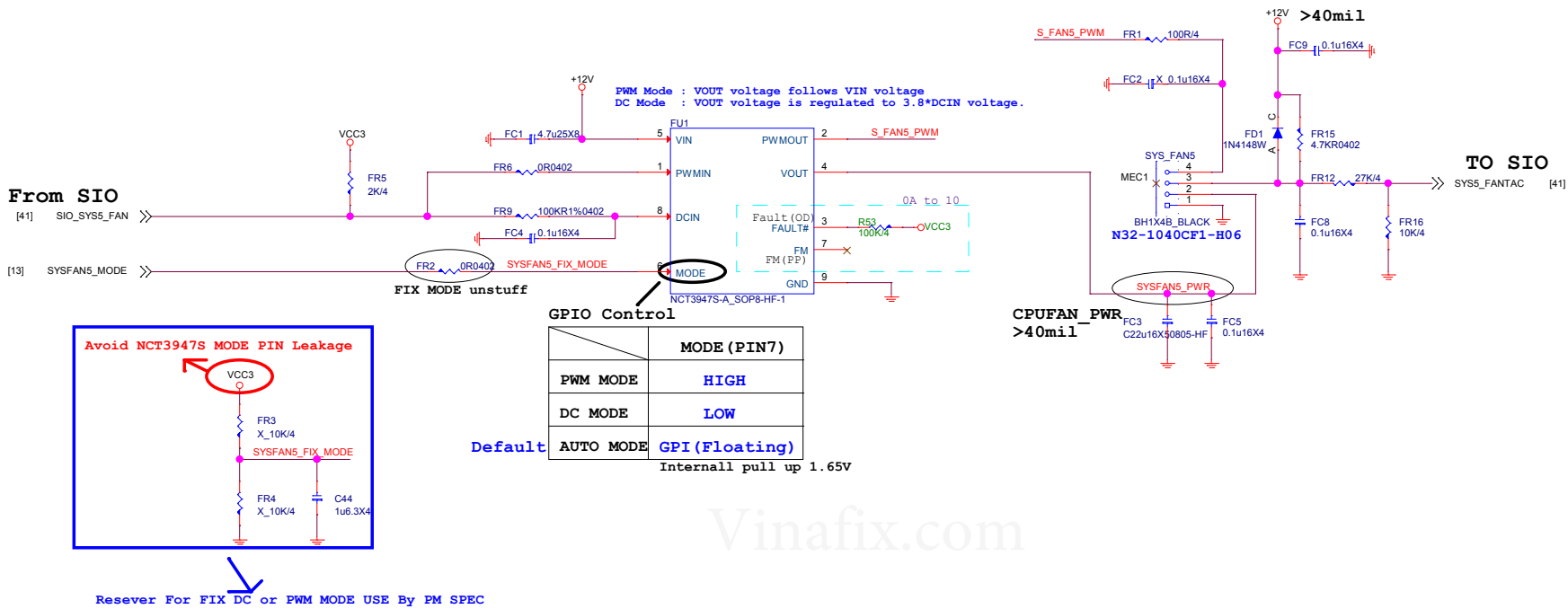
2. GPIO可以由BIOS切換 PWM/DC MODE



GPIO Control	
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPIO(Floating)

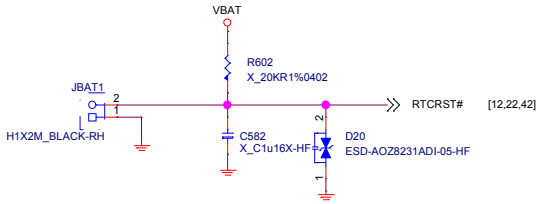
Internall pull up 1.65V

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



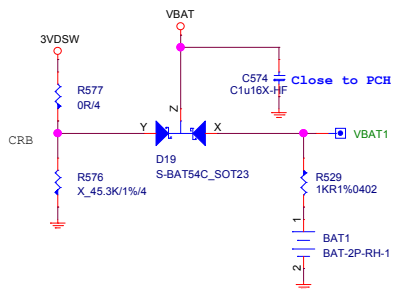
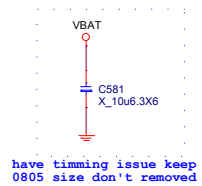
Delete ALL Audio LED BY Spec Change 2018/4/19

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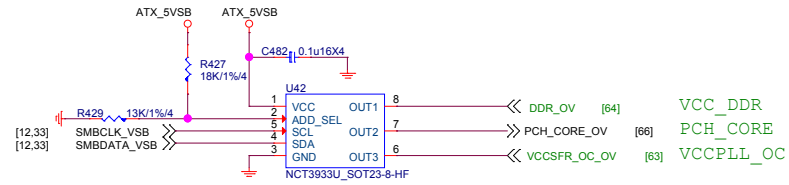
VBAT



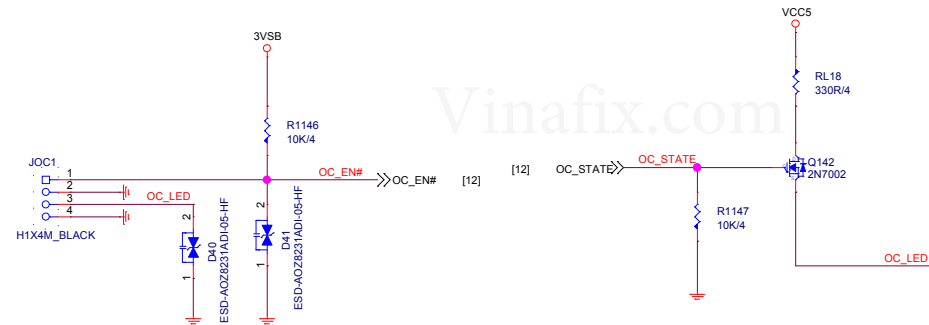
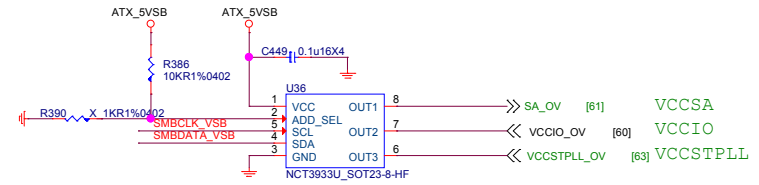
0x20: RH=10K, RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPE
BUS_SEL	0%	25%	40%	60%	75%	100%

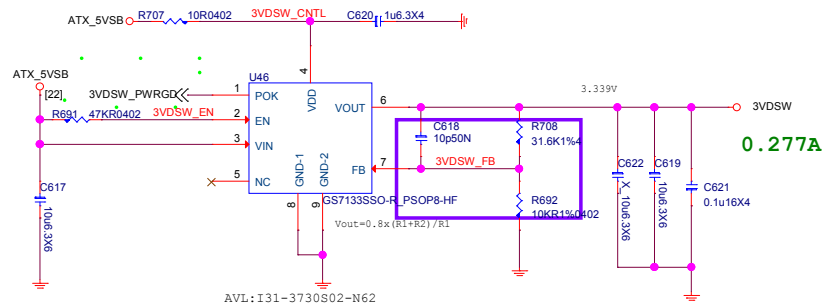
0x26: RH=18K, RL=13K



0x20: RH=10K, RL=OPEN

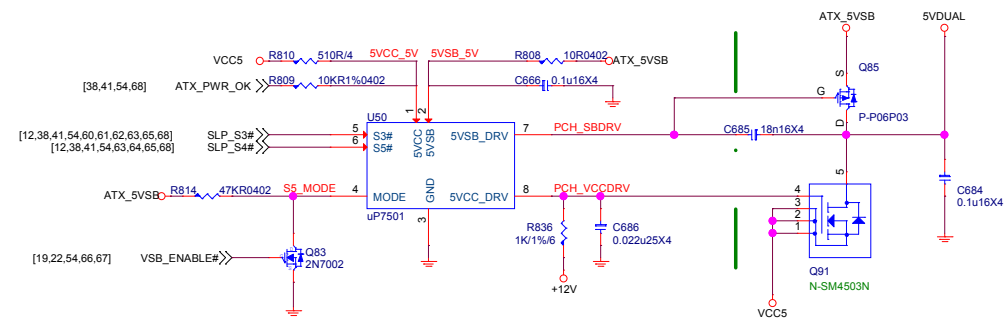


3VDSW



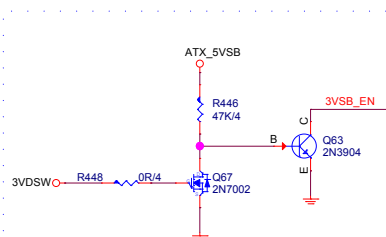
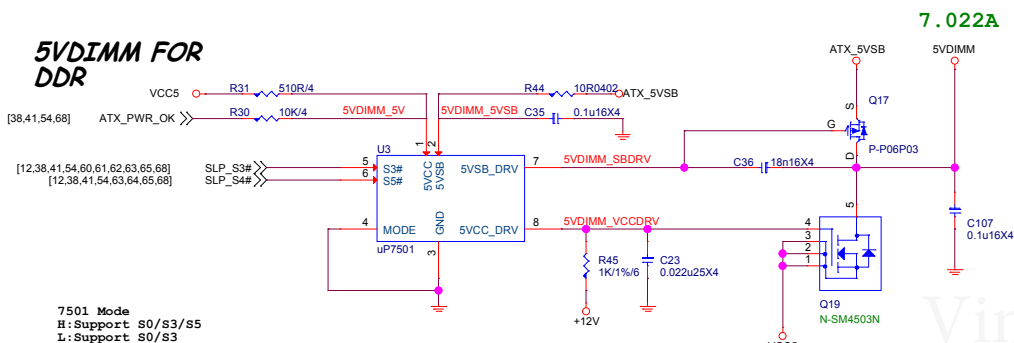
5VDUAL

5VDUAL is power source of 1P0SB

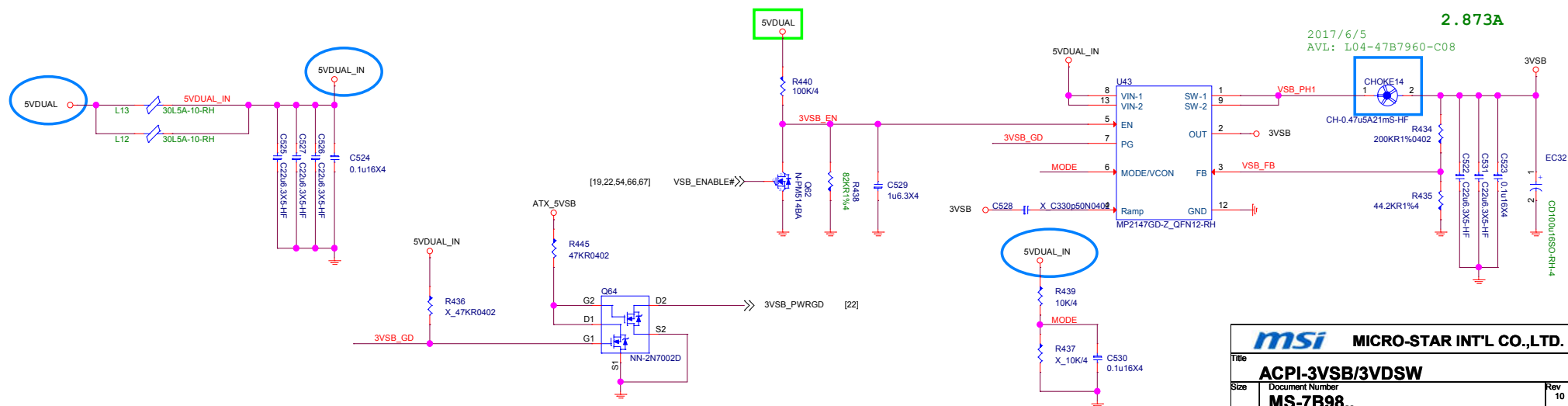


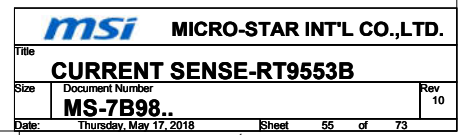
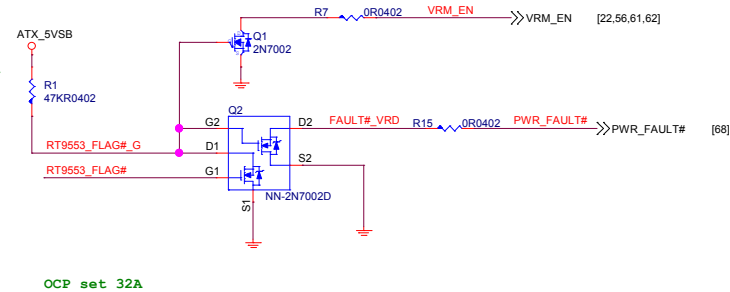
Change to discrete type
2018/1/18

5VDIMM FOR DDR

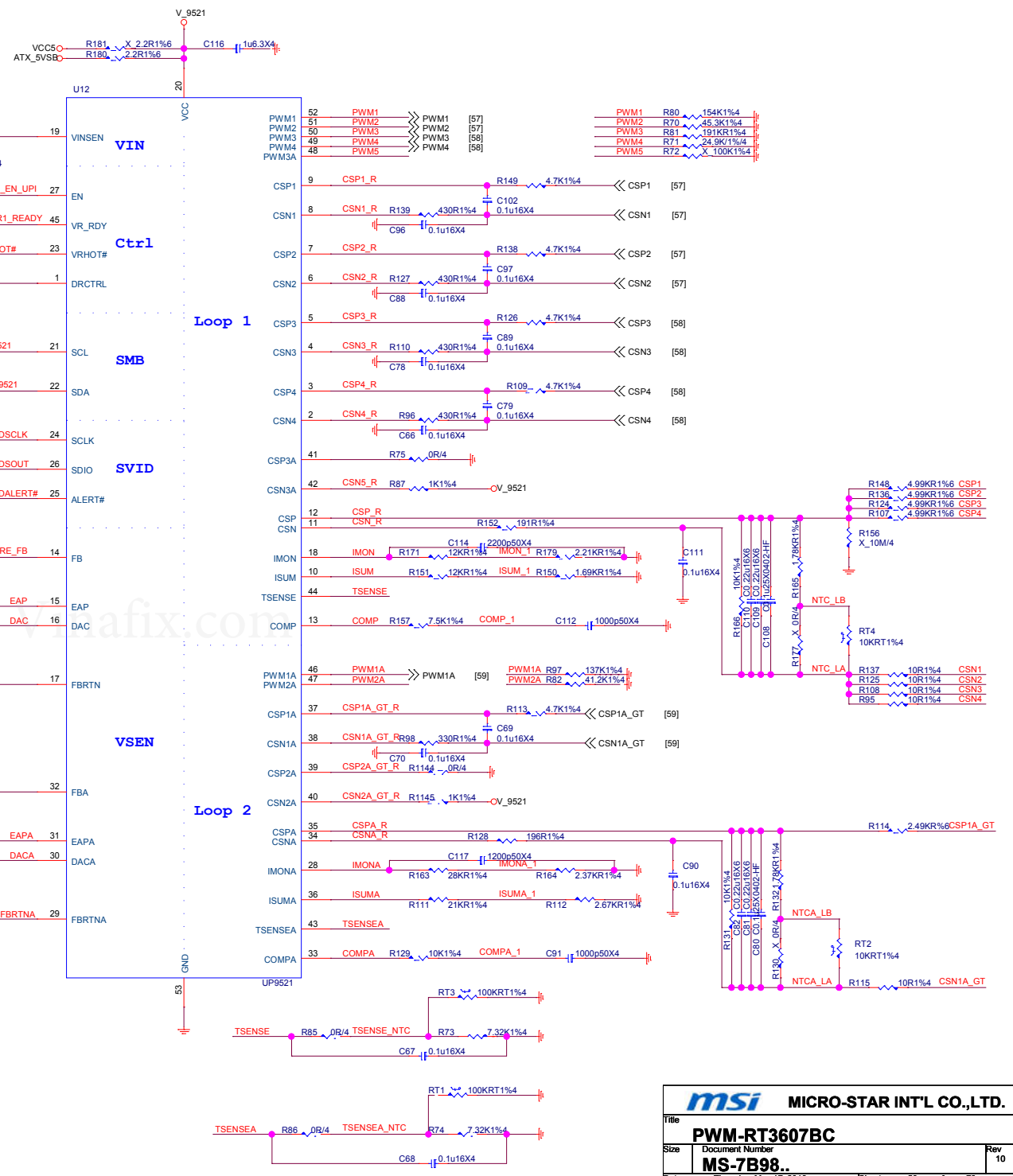
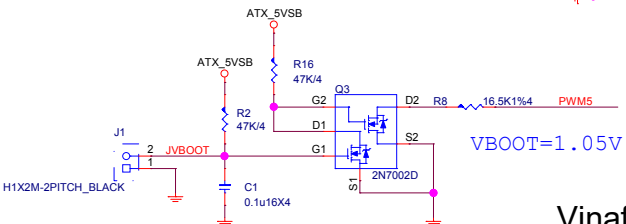


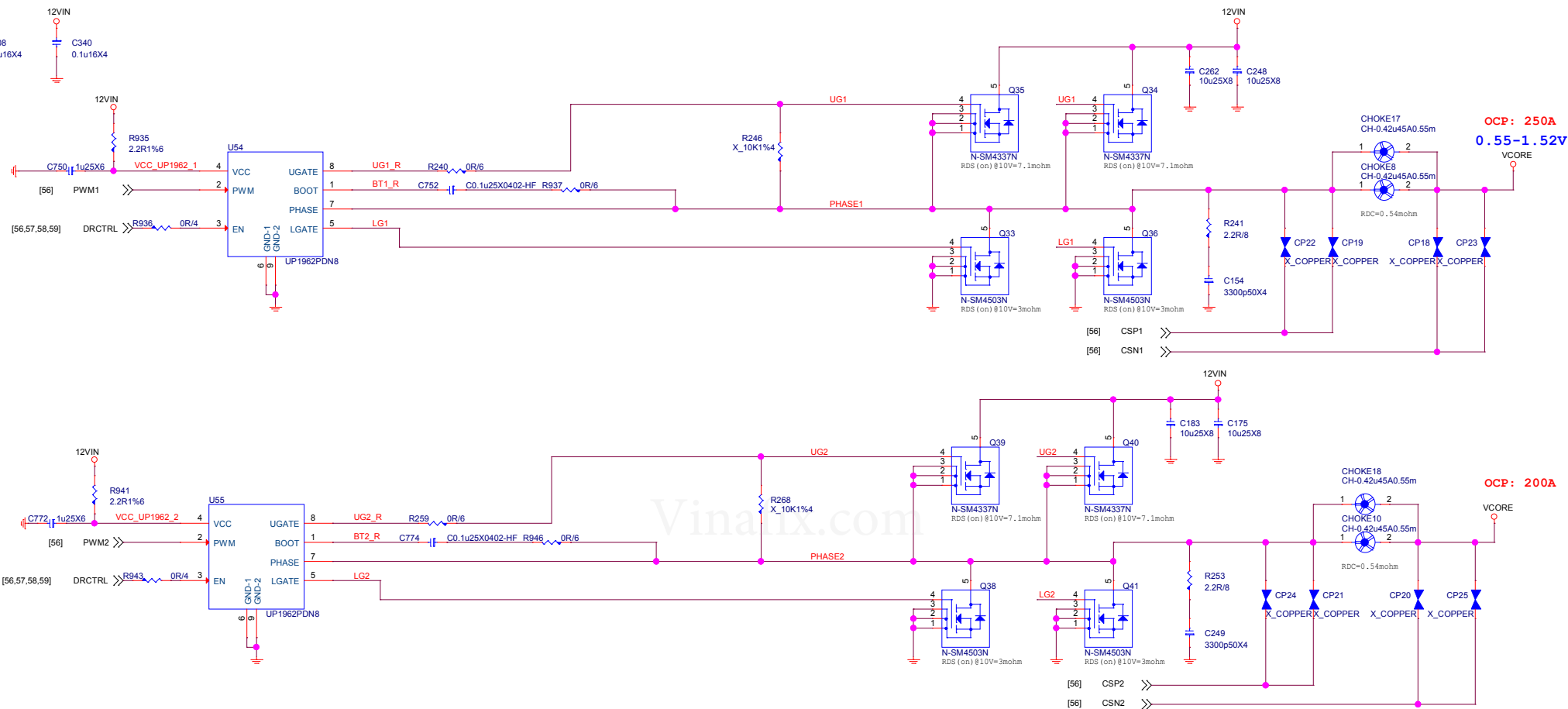
for S5-G3 3VSB EN ISSUE



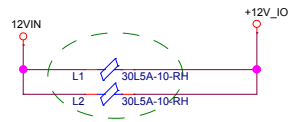


VGT: ICC Max 45A
LL: 3.1 mohm
OCP: 75A(Per-Phase)*1Phase=75A





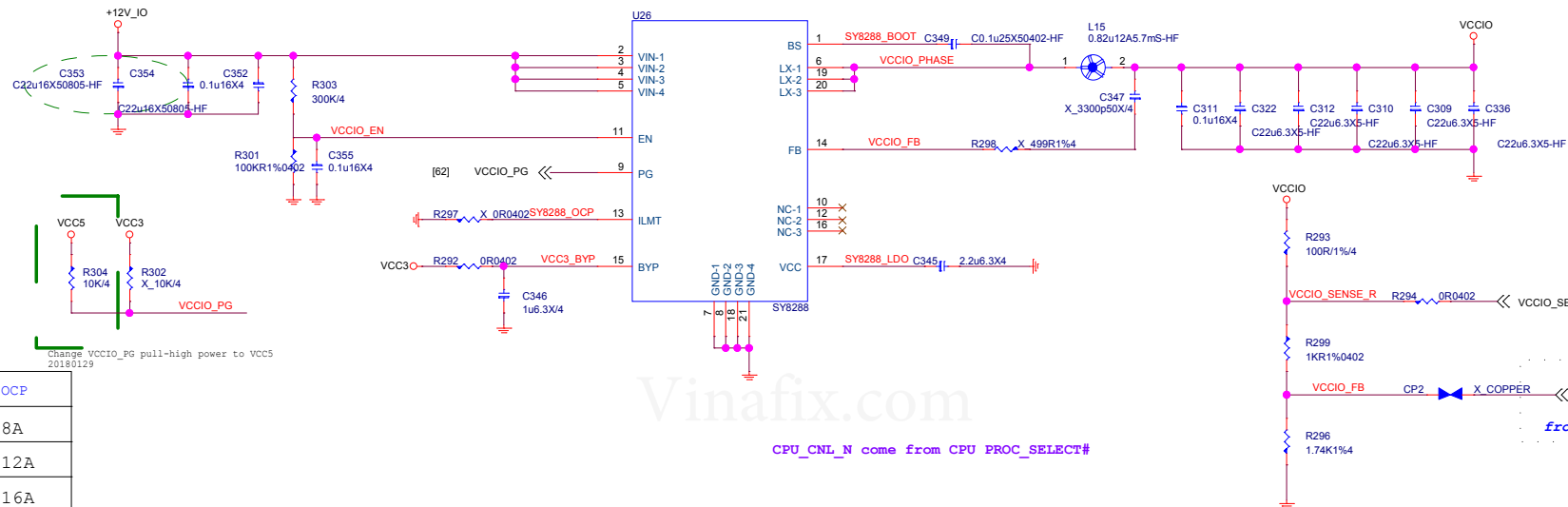
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.



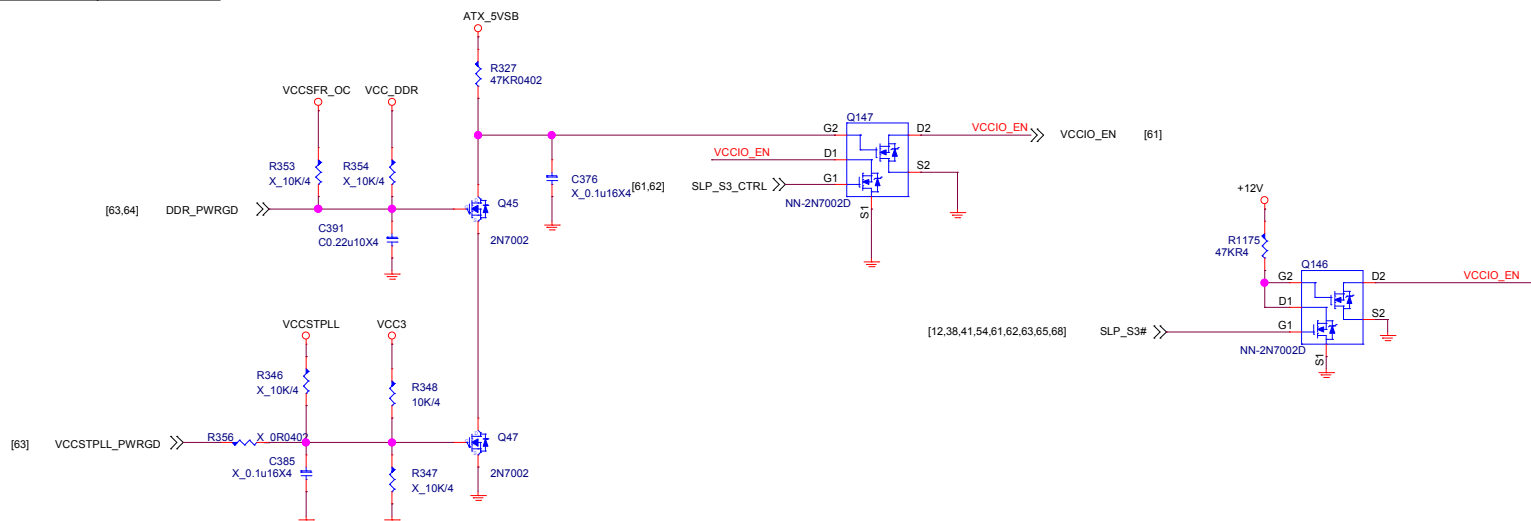
```

95W
ICCMAX=6.4A
Irms = 1.728A

```



SY8288_OCP	OCP
0	8A
floating	12A
1	16A



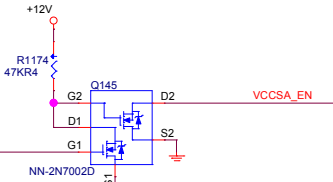
SA Power:1.05V

1.05V; 11.1A

OCp = 11.1*1.4=15.54A
 Rocset = 1.4 * Imax * Rdson(low) / Iocset
 = 1.4 * 11.1 * 3.3mohm / 10uA
 = 5.12K (BOM 5.1K)

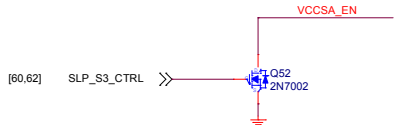
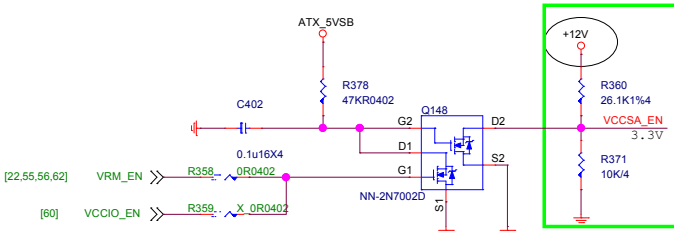
Rdson(low) 10V
 D03-4503N0C-ST8 : 3mohm

2014.12.25
 for up1540:C39 is OCP set min:5K ohm
 stuff 5.36K OCP SET:15.76A



2014.08.21 update

Pull up by layout&Check level

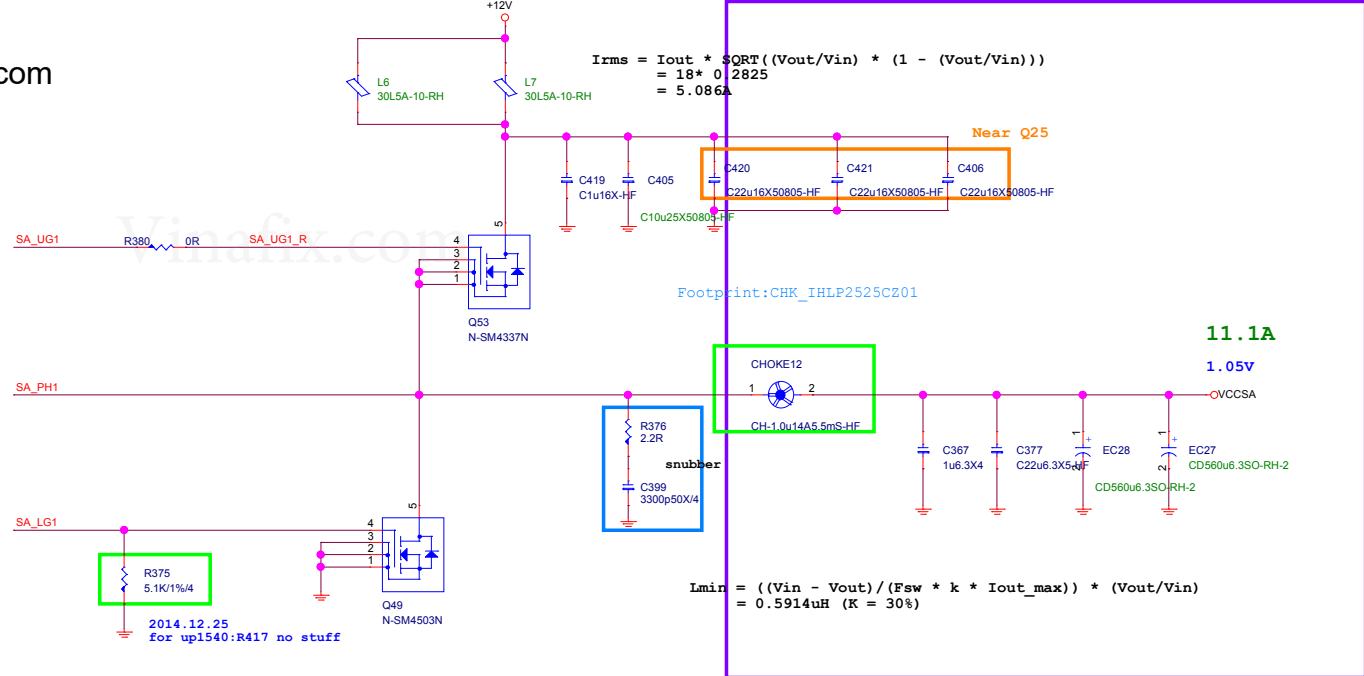
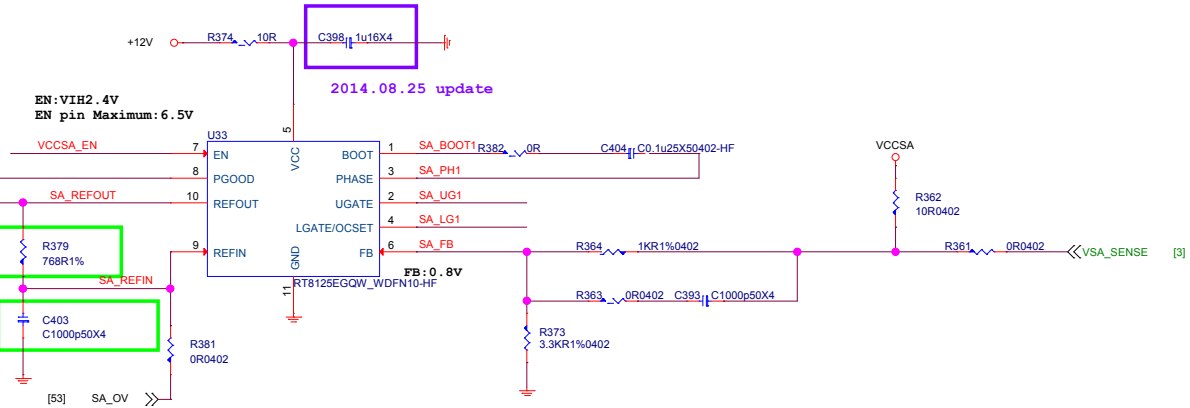


SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
 max:1us

EN:VIH2.4V
 EN pin Maximum:6.5V

Vinafix.com



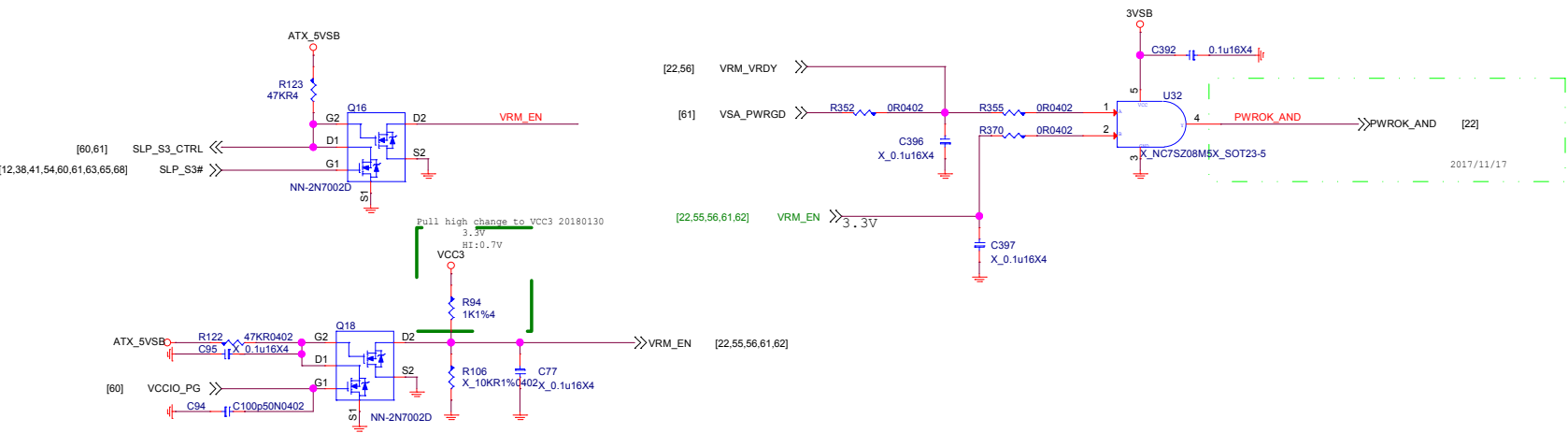
Footprint:CHK_IHLP2525C201

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
 = 0.5914uH (K = 30%)

msi MICRO-STAR INT'L CO.,LTD.

CPU PWR-VCCSA-RT8125E			Rev
Size	Document Number	MS-7B98..	10
Date:	Thursday, May 17, 2018	Sheet	61 of 73

Sequence

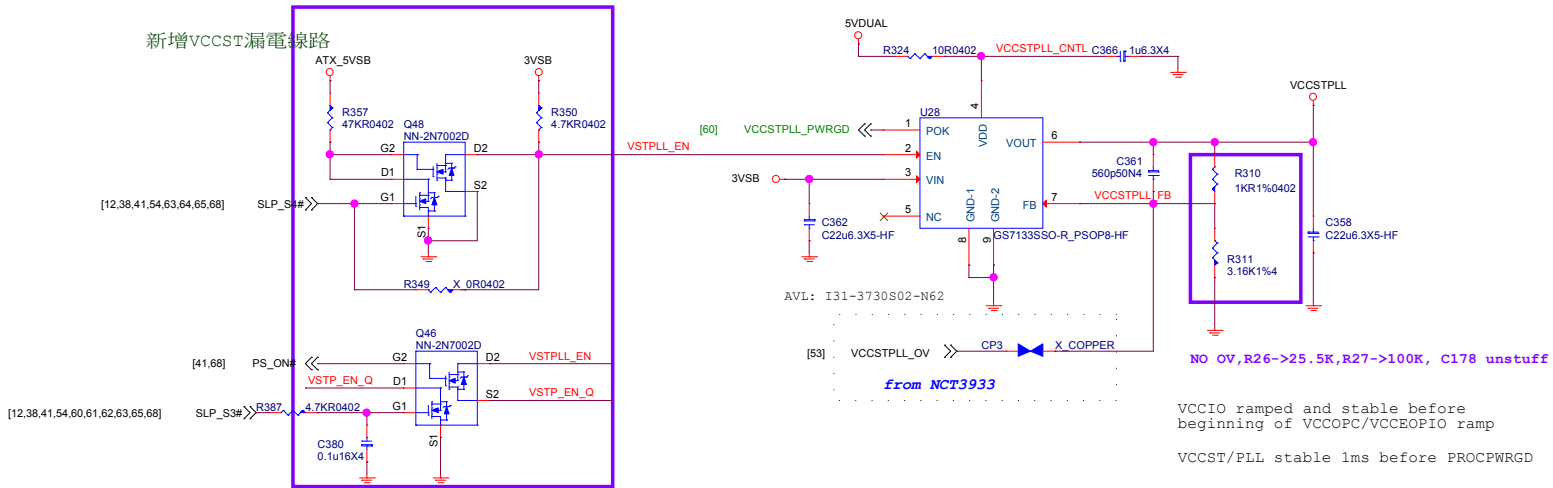


Vinafix.com

VCCSTPLL

1.05V; 230mA

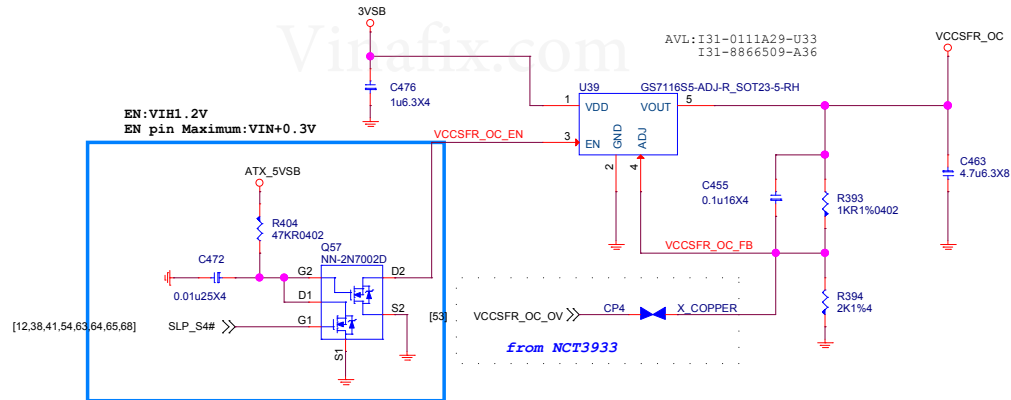
For Cost down VCCST&VCCPLL merge



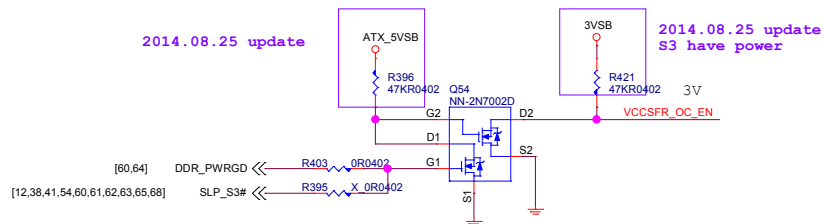
VCCPLL OC

1.2V; 130mA

2014.08.21 update



2014.08.25 update



2014.08.25 update
S3 have power

DDR4_1.2V 19.5A

OCp 27.58

Vinafix.com

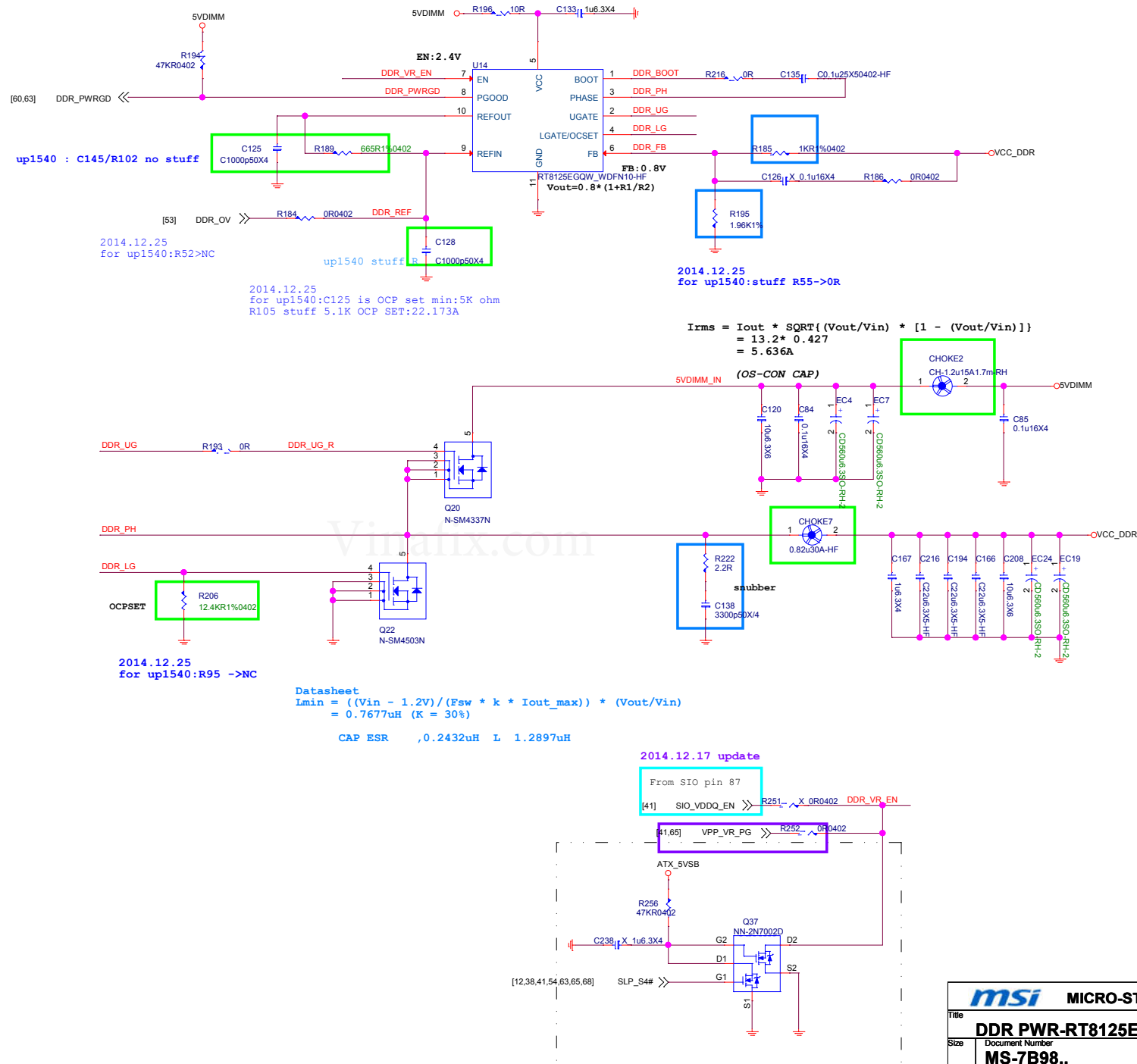
3.3A FOR
CPU

15.7A FOR
4DIMM

0.5A FOR DDR
VTT

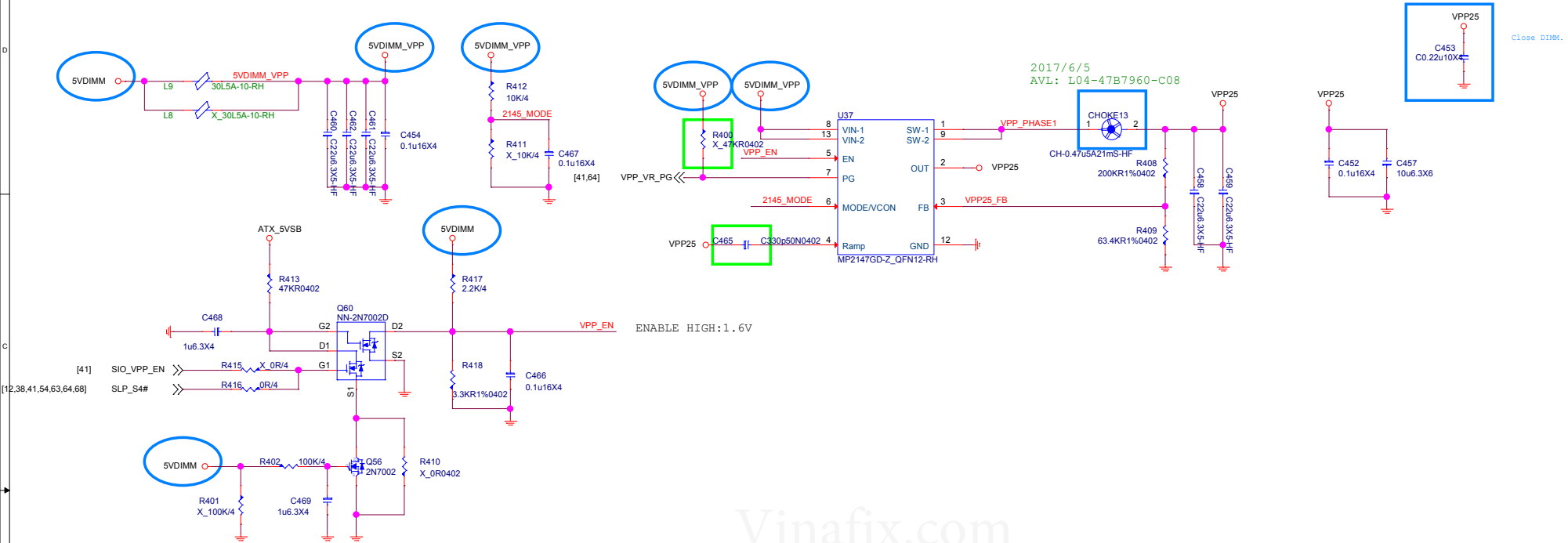
OCp = 19.7*1.4=27.58A

Rocset = 1.4 * I_{max} * R_{ds(on)}(low) / I_{ocset}
= 1.4 * 19.5 * 4.6mohm / 10uA
= 12.6K (BOM 12.4K)



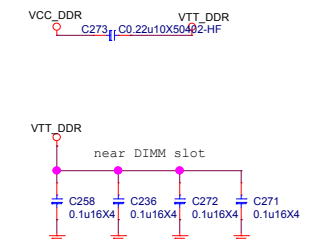
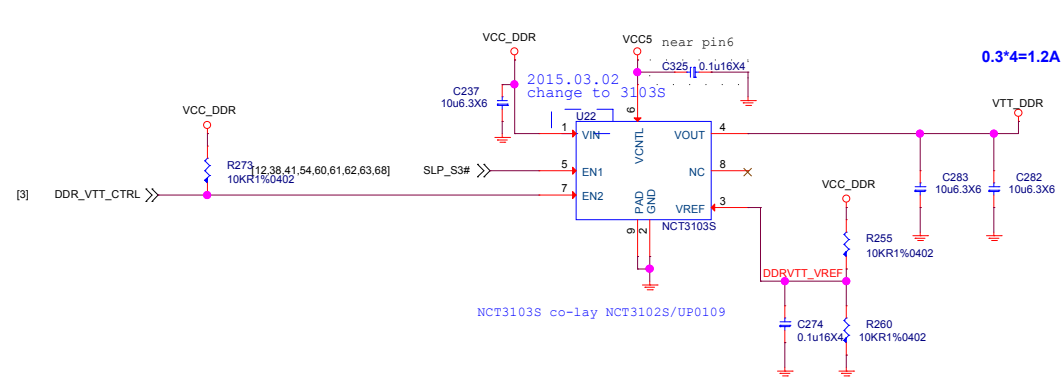
4DIMM :2.24A FOR
DDR VPP2.5V

VPP25 Power
2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

DDR VTT Power



PCH 1VSB

1.05V; 13.36A

Rdson(10V) 4.5V
D03-3116M00-U47 : 3.6 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

OCP = 13.36*1.4=18.704A

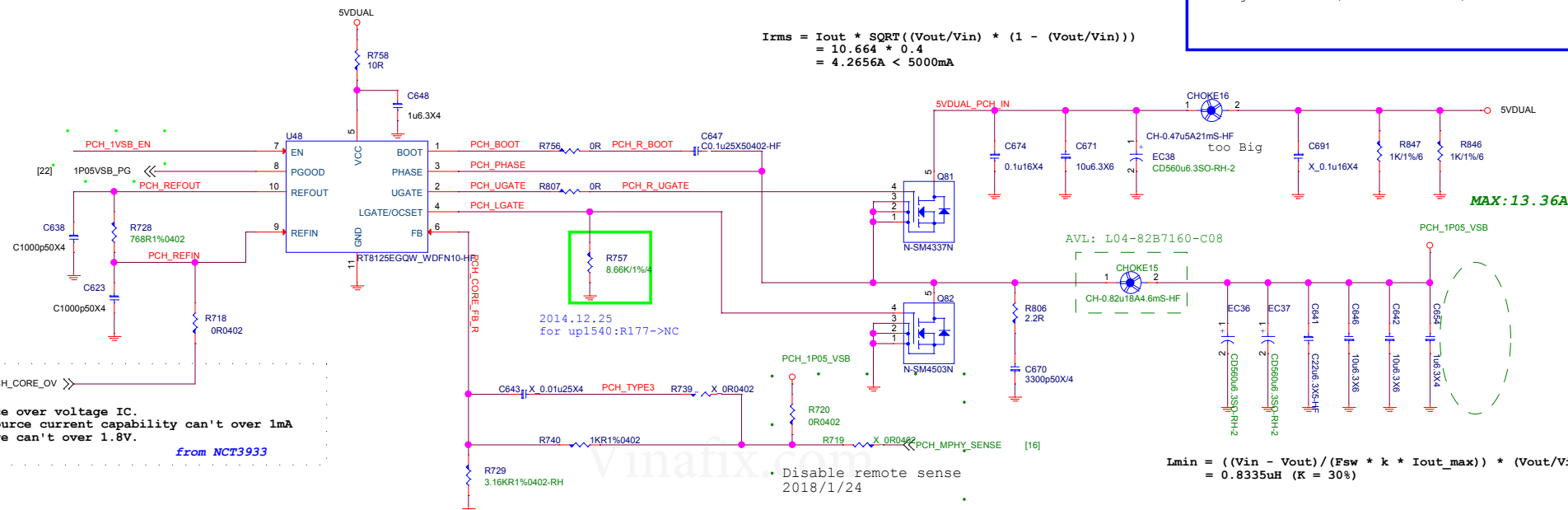
Rocset = 1.4 * I_{max} * Rdson(10V) / Iocset
= 1.4 * 13.36 * 4.6mohm / 10uA
= 8.6K (BOM 8.66K)

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

Change to Choke (L04-47B7930-M26) form bead



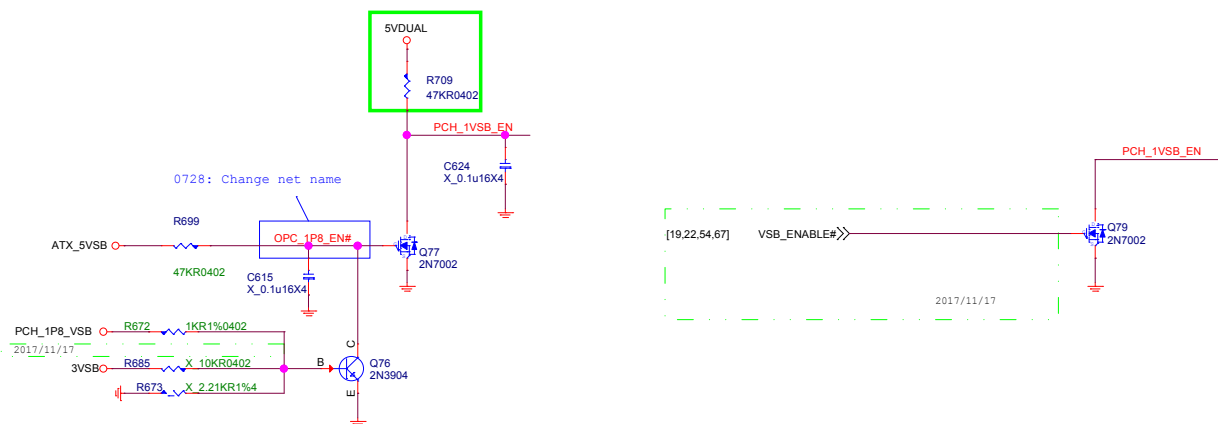
$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

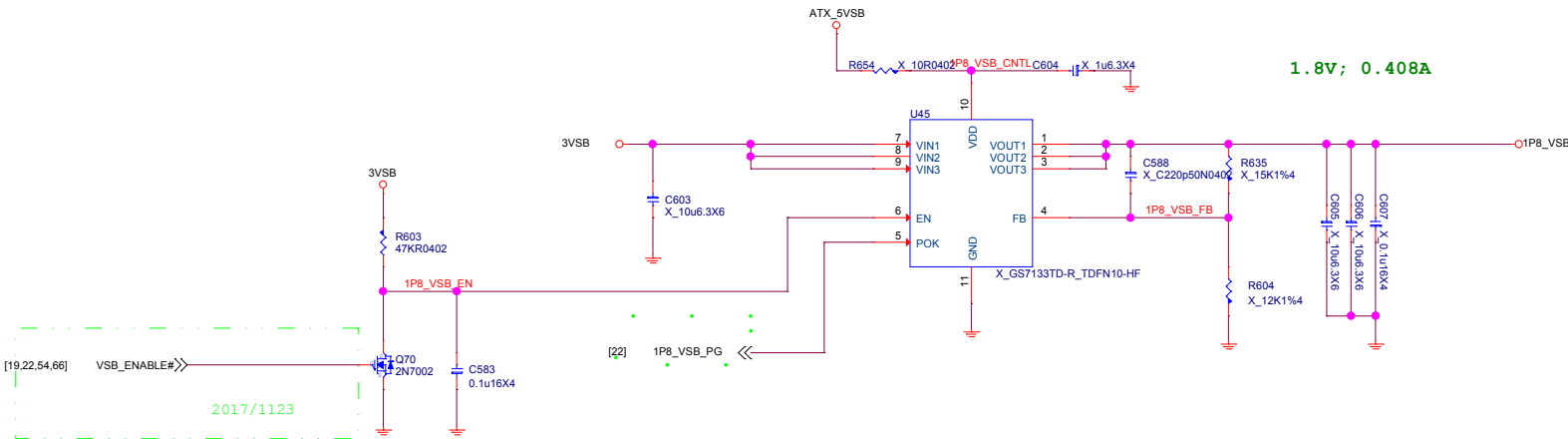
$$= 0.8335uH (K = 30\%)$$

to sink/source over voltage IC.
pin10 sink/source current capability can't over 1mA
So max voltage can't over 1.8V.

from NCT3933

Vinafix.com



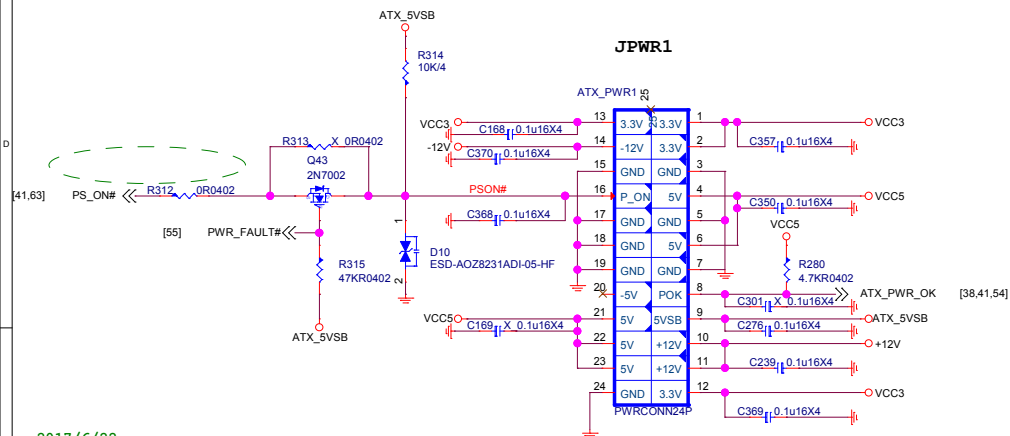


Delete due to USB retimer use external DC to DC schematic
2018/01/17

Vinafix.com

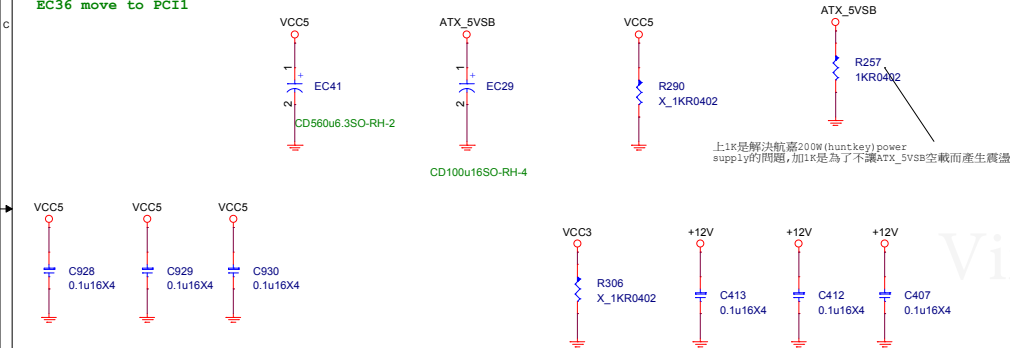
ASM_1P8_VSB Delete ,due to drop ASM 1562

ATX POWER CONNECTOR

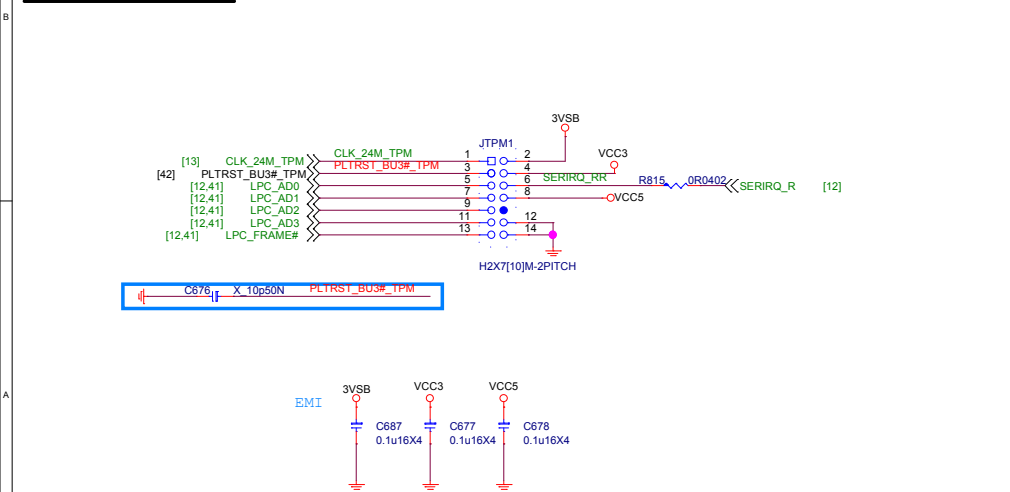


2017/6/22
EC34, EC36 are changed from 470uF to 560uF by buyer request

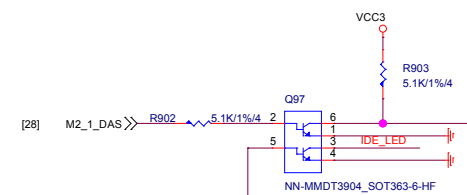
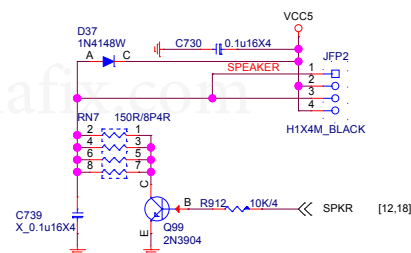
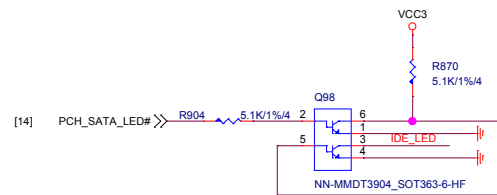
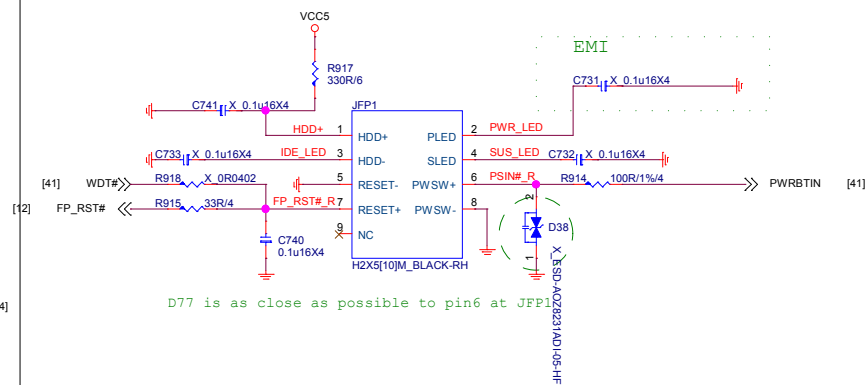
2017/7/6
EC36 move to PCI1



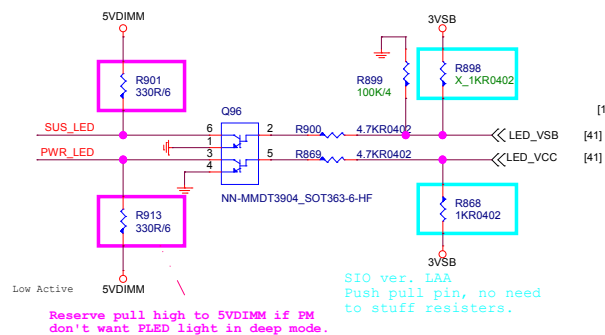
TPM Pin Header



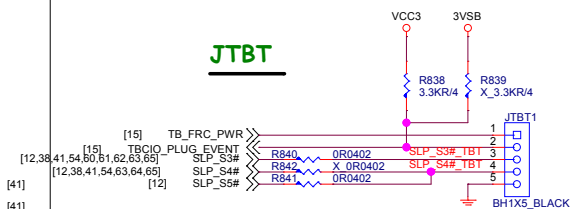
FRONT PANNEL



Front Panel
LED

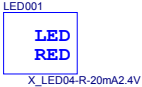
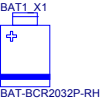


JTBT

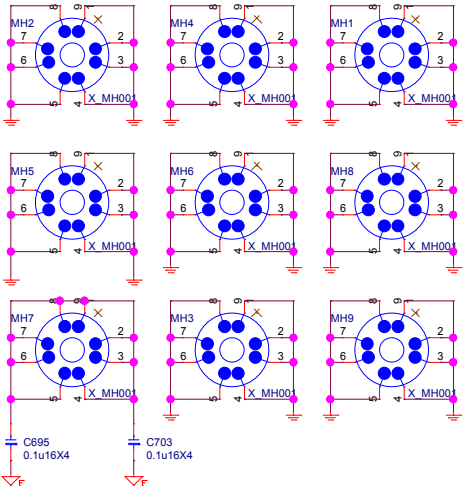




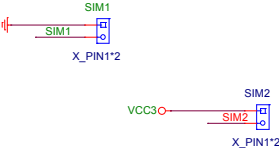
PK0-07B980A-G37, 精成-深圳, 23, 寶安恩斯邁廠 (MSIS)
PK0-07B980A-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)



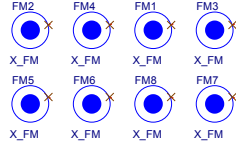
Mounting Holes



Simulation



Optical Fiducial Marks-120



Vinafix.com

Vcheck

